清光緒年間臺灣全圖

Digital Integrated Circuits

A Design Perspective

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The Devices

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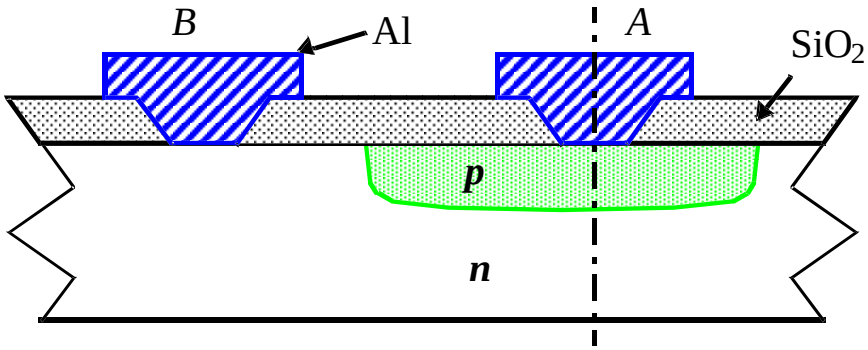
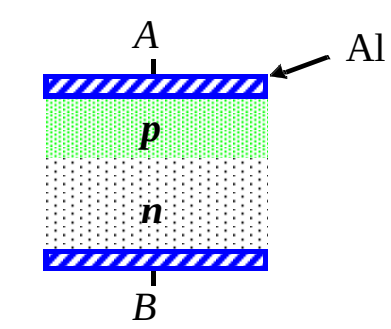
Goal of this chapter

- Present intuitive understanding of **device operation**
- Introduction of **basic device equations**
- Introduction of **models for manual analysis**
- Introduction of models for **SPICE simulation**
- Analysis of secondary and **deep-sub-micron effects**
- **Future trends**

The Diode

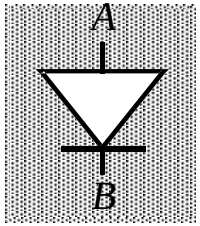


Cross-section of *pn* -junction in an IC process



One-dimensional representation

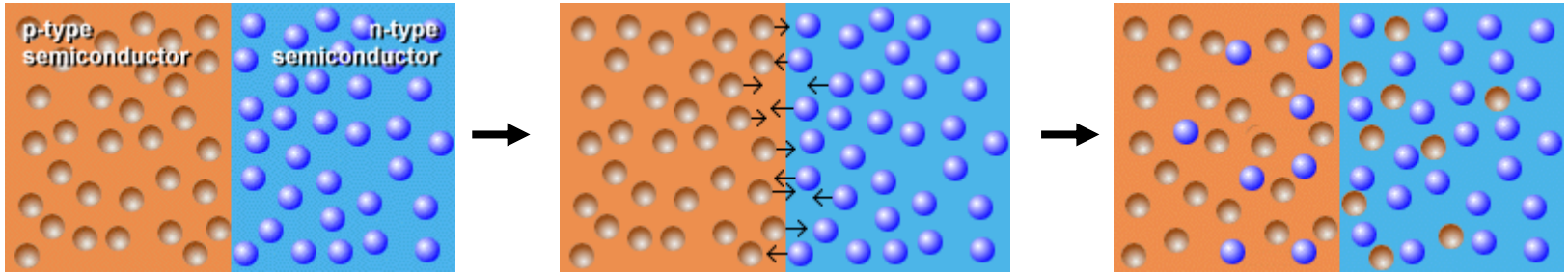
假設 Al 爲超導體 → R = 0



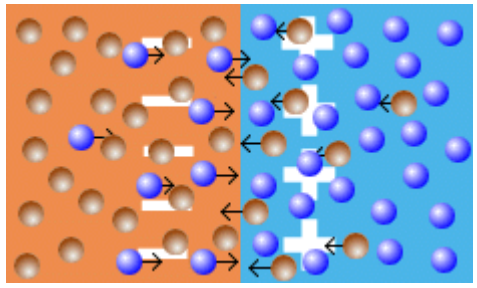
diode symbol

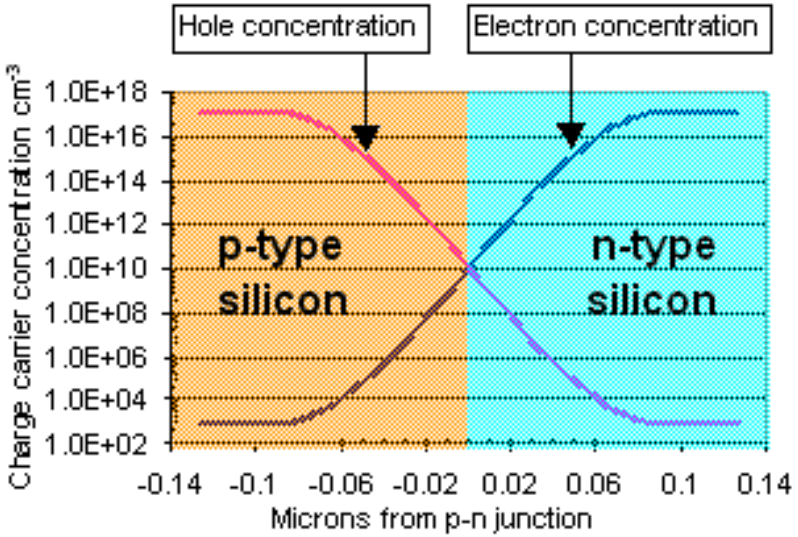
Mostly occurring as parasitic element in Digital ICs

PN Junction

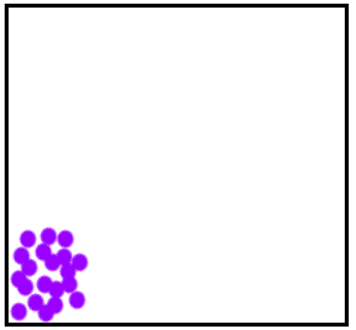


Charge carriers
- Free electron
- Electron hole





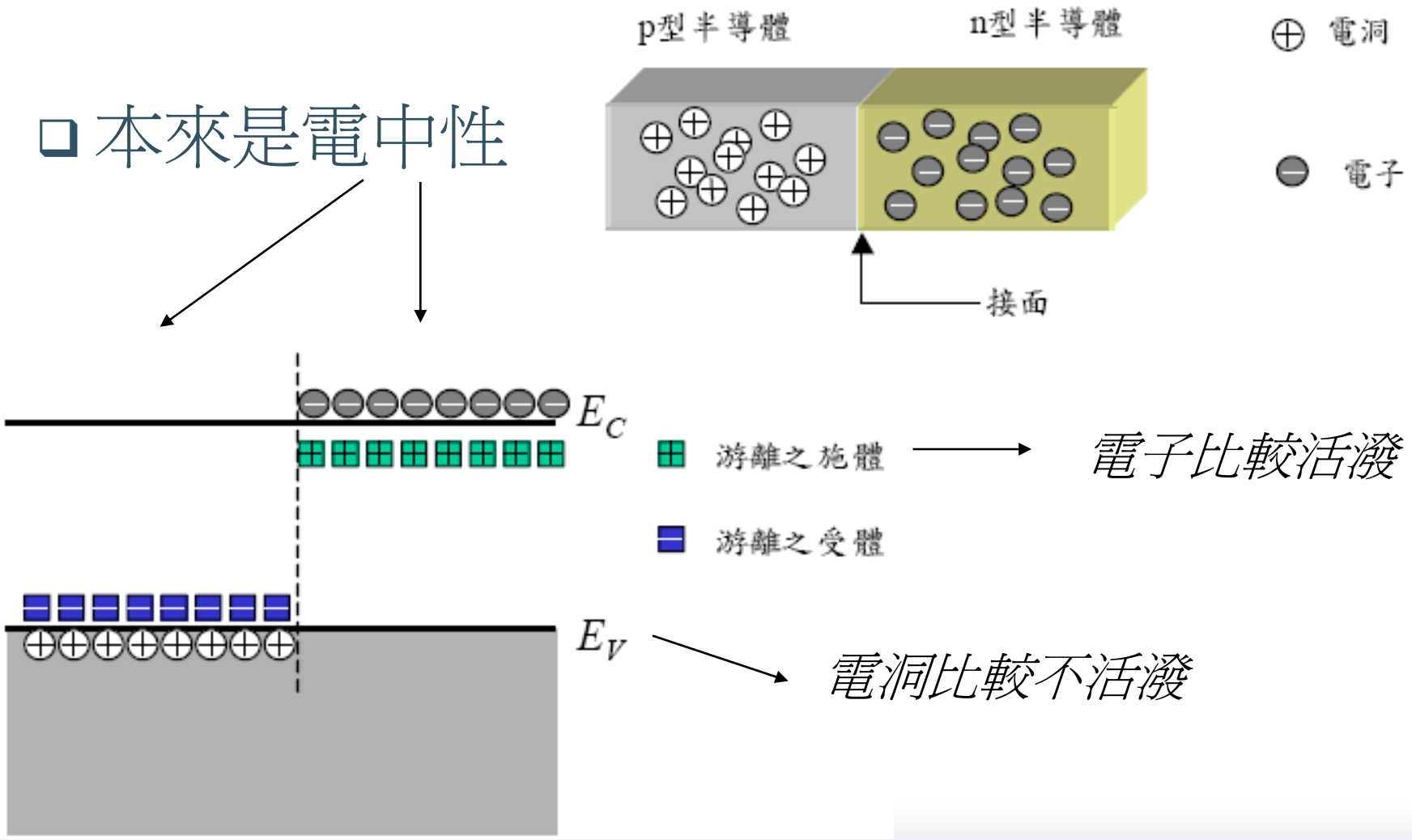
Diffusion Current vs. Drift Current



- Diffusion current
  - Random motion
  - Occurs at all times and places
  - Resembles Brownian motion
  - From high concentration to low concentration
- Drift current
  - Unidirectional movement
  - By electric field

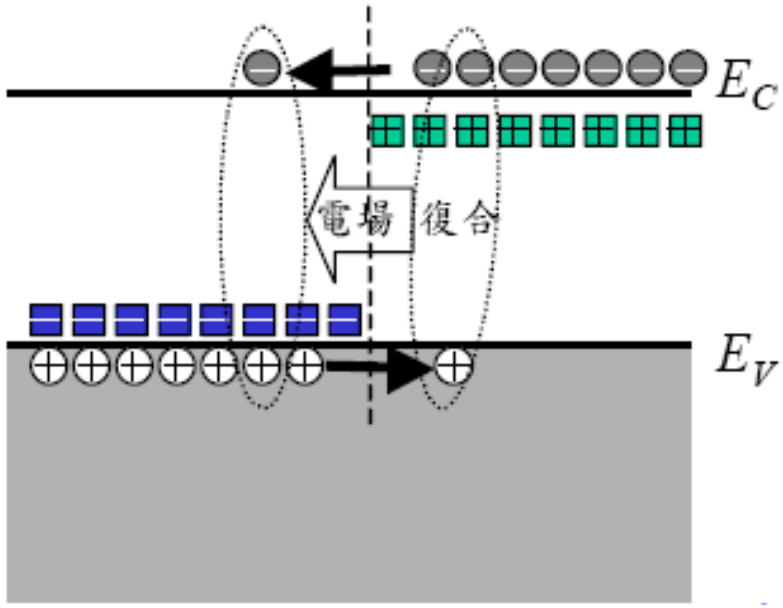
What is Depletion Region ? (1/4)

- 本來是電中性

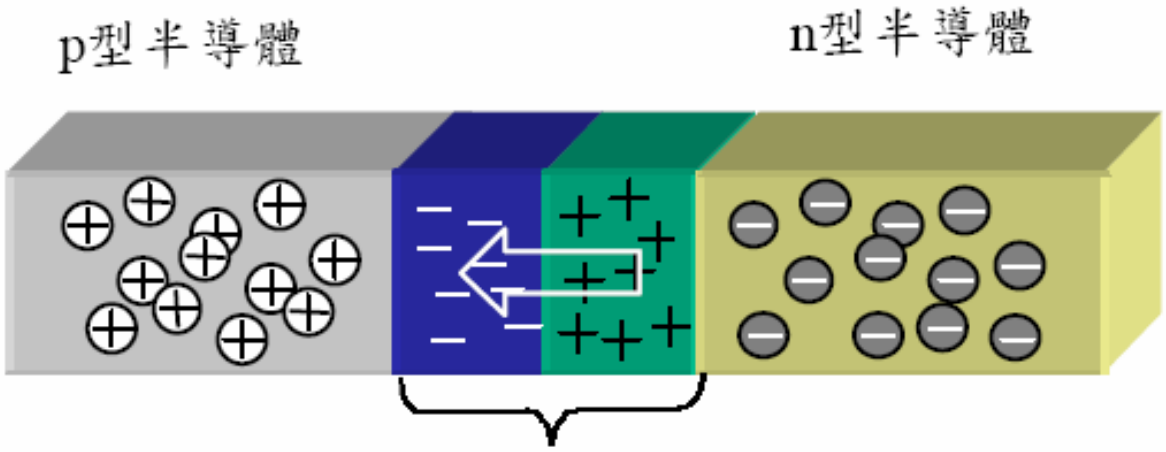


What is Depletion Region ? (2/4)

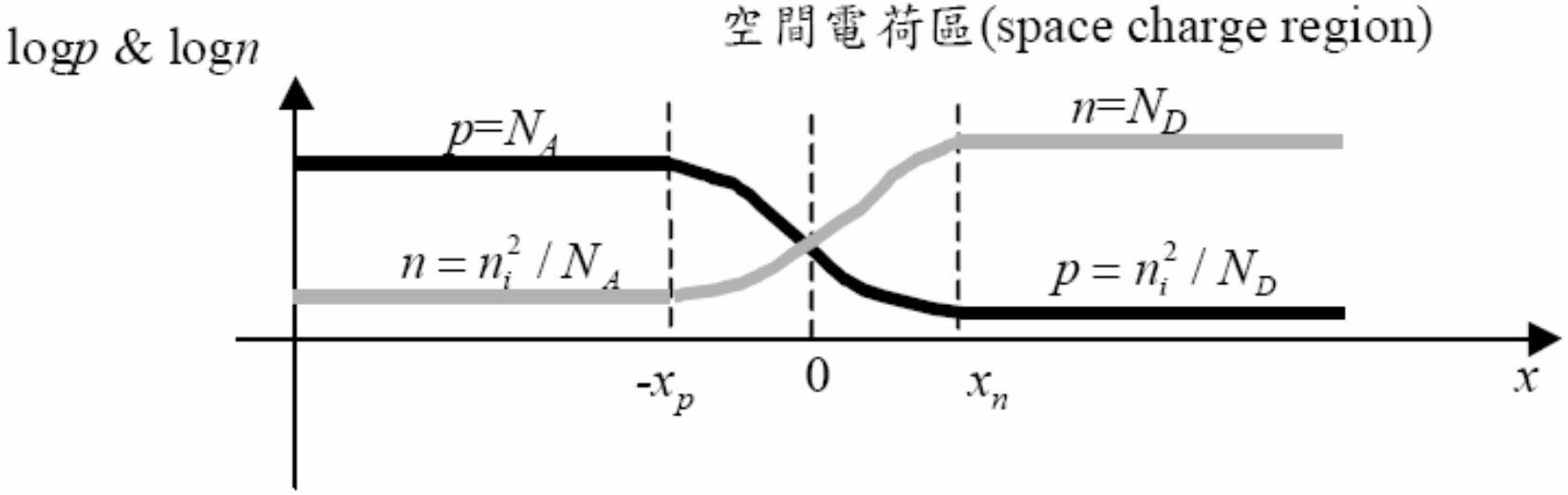
- 因爲左右兩端濃度 (Concentration) 不均
  - → 開始移動
  - → 電中性破壞了



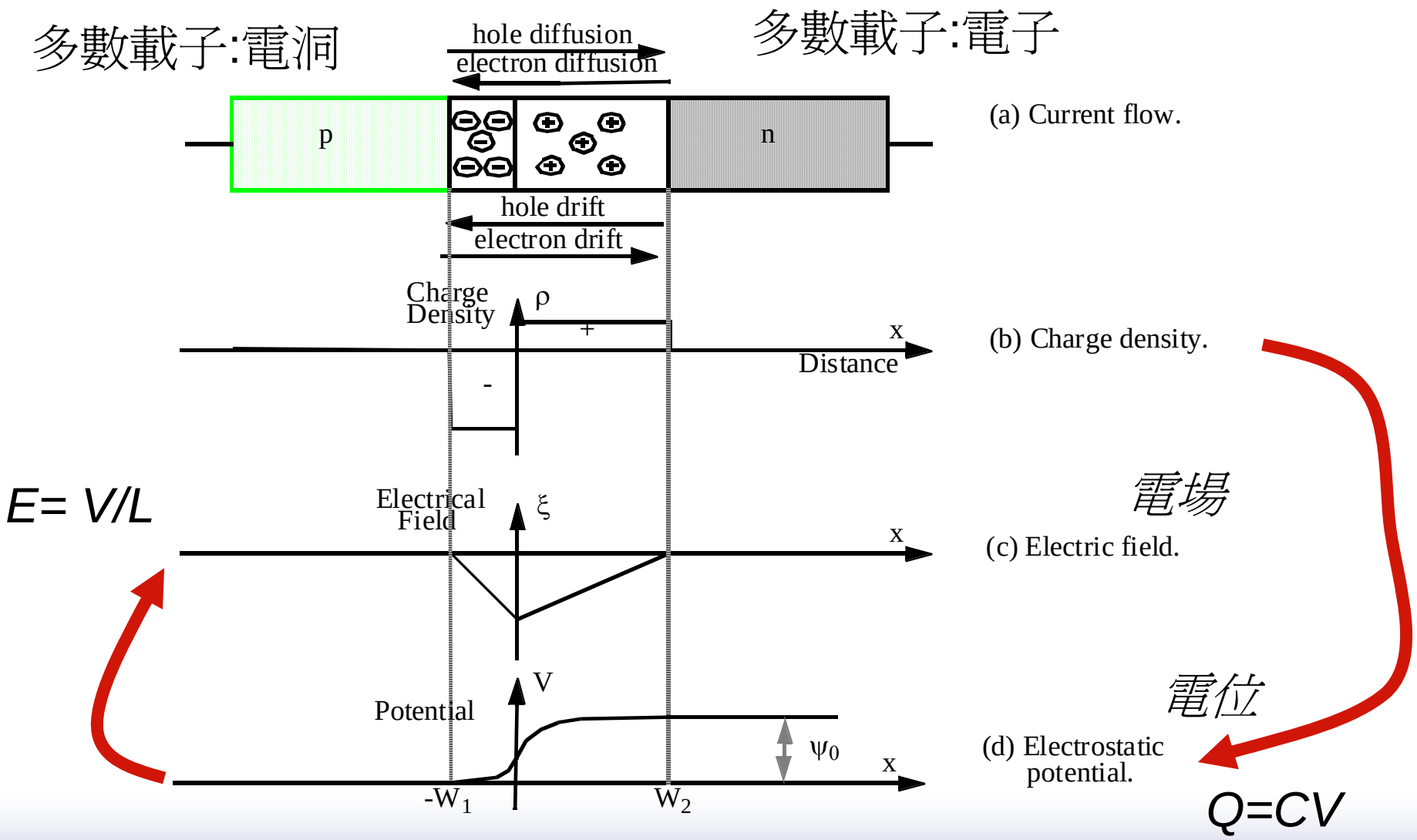
What is Depletion Region ? (3/4)



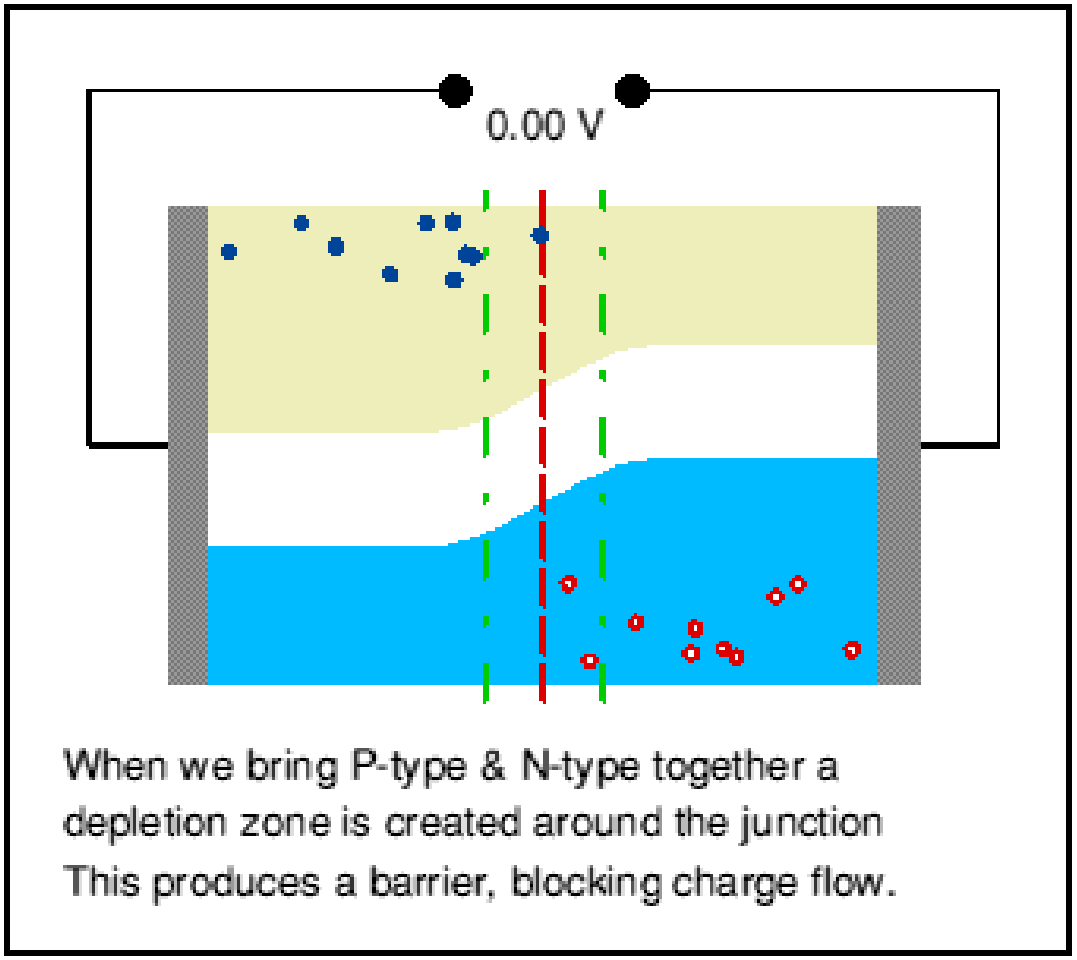
空乏區(depletion region)
空間電荷區(space charge region)



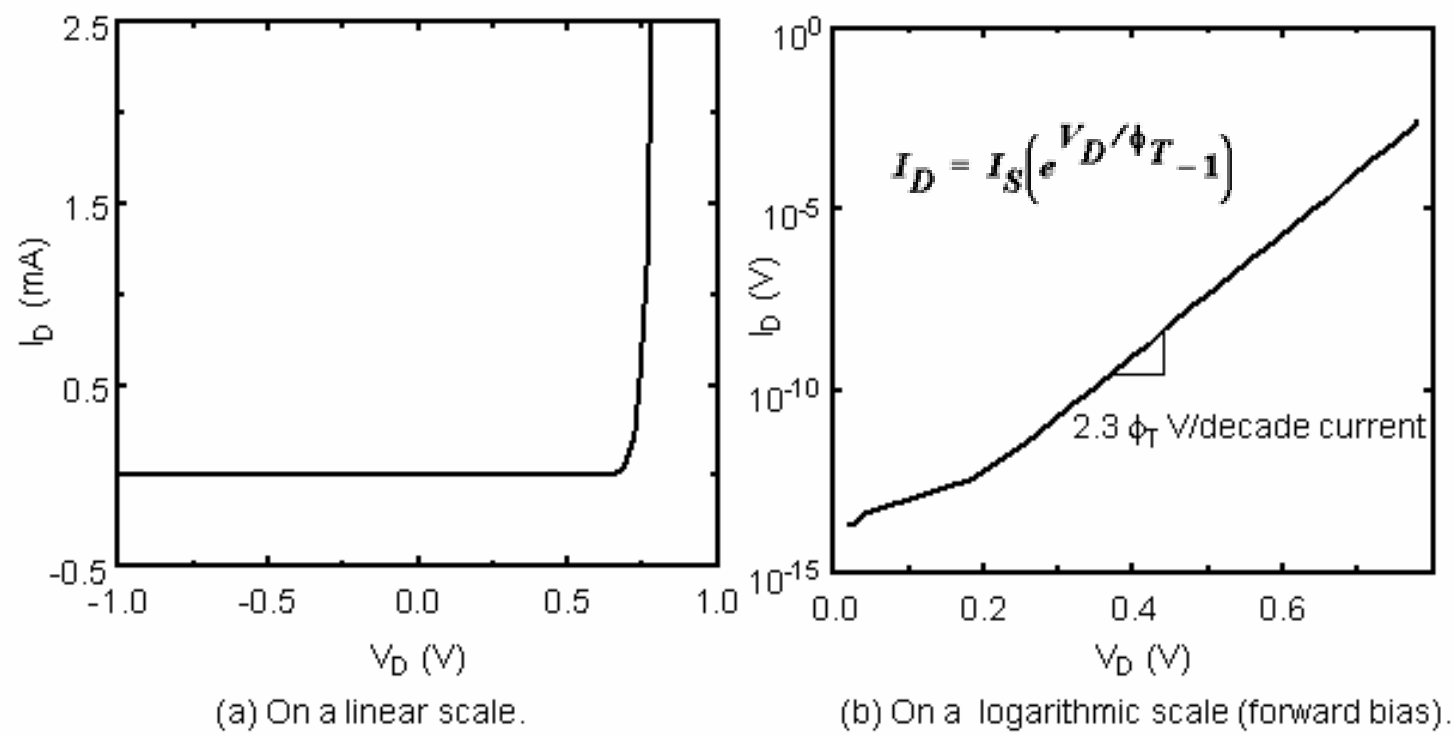
What is Depletion Region ? (4/4)



An Animation



Diode Current



(a) On a linear scale.

(b) On a logarithmic scale (forward bias).

$$I=I_o(e^{qv/kT}-1)$$

式中 I_o 爲反向飽和電流，q爲基本電荷量，k 爲波茲曼常數，T 爲絕對溫度。

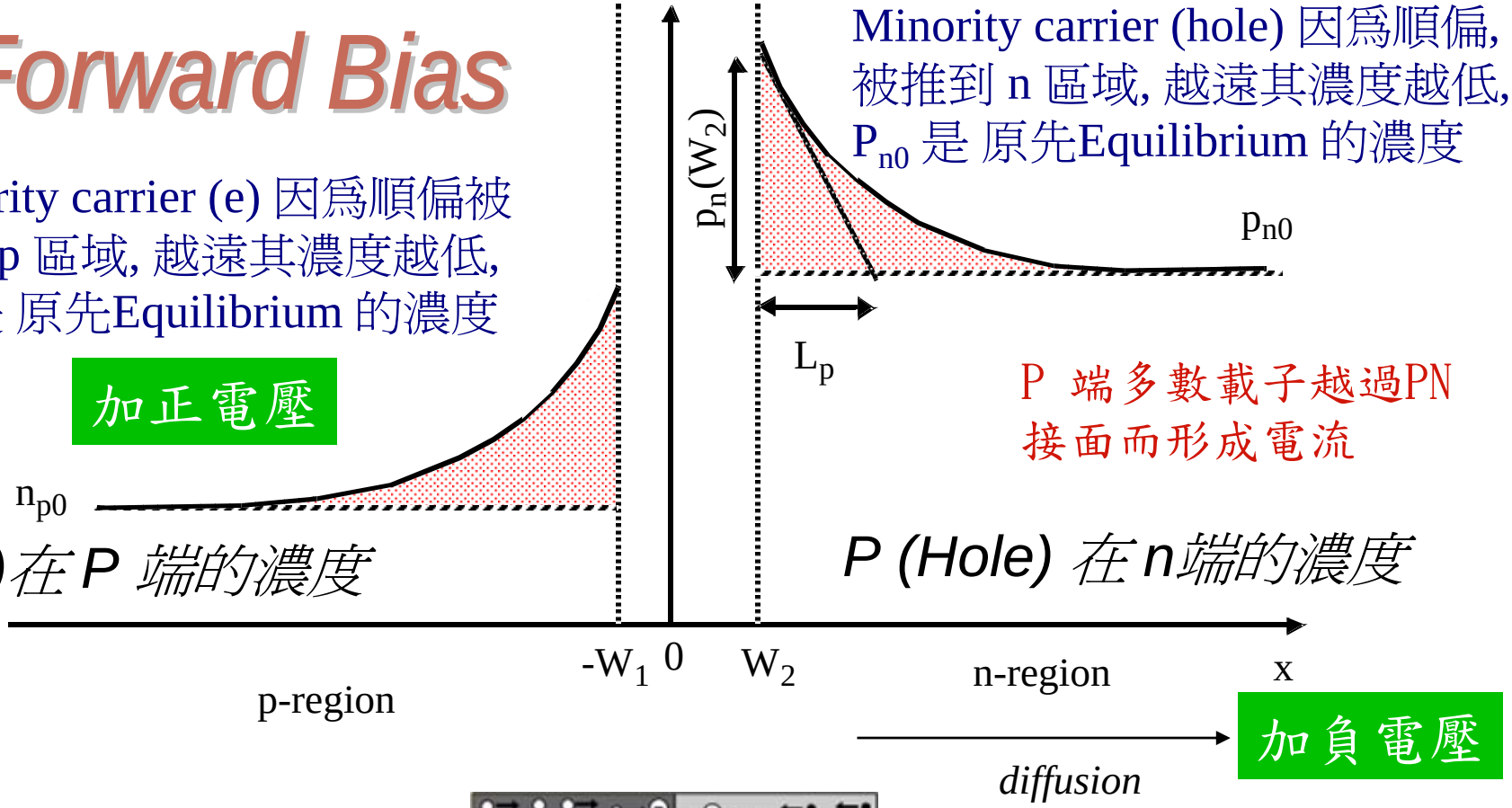
Forward Bias

Minority carrier (e) 因爲順偏被吸到 p 區域, 越遠其濃度越低, n_{p0} 是 原先Equilibrium 的濃度

加正電壓

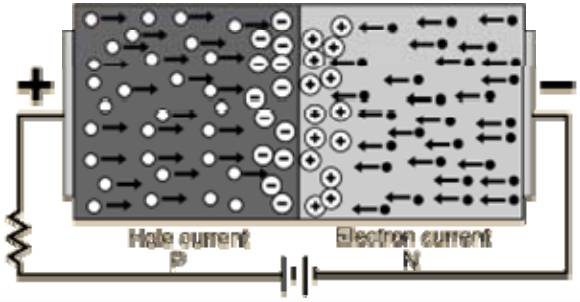
Minority carrier (hole) 因爲順偏, 被推到 n 區域, 越遠其濃度越低, P_{n0} 是 原先Equilibrium 的濃度

P 端多數載子越過PN接面而形成電流



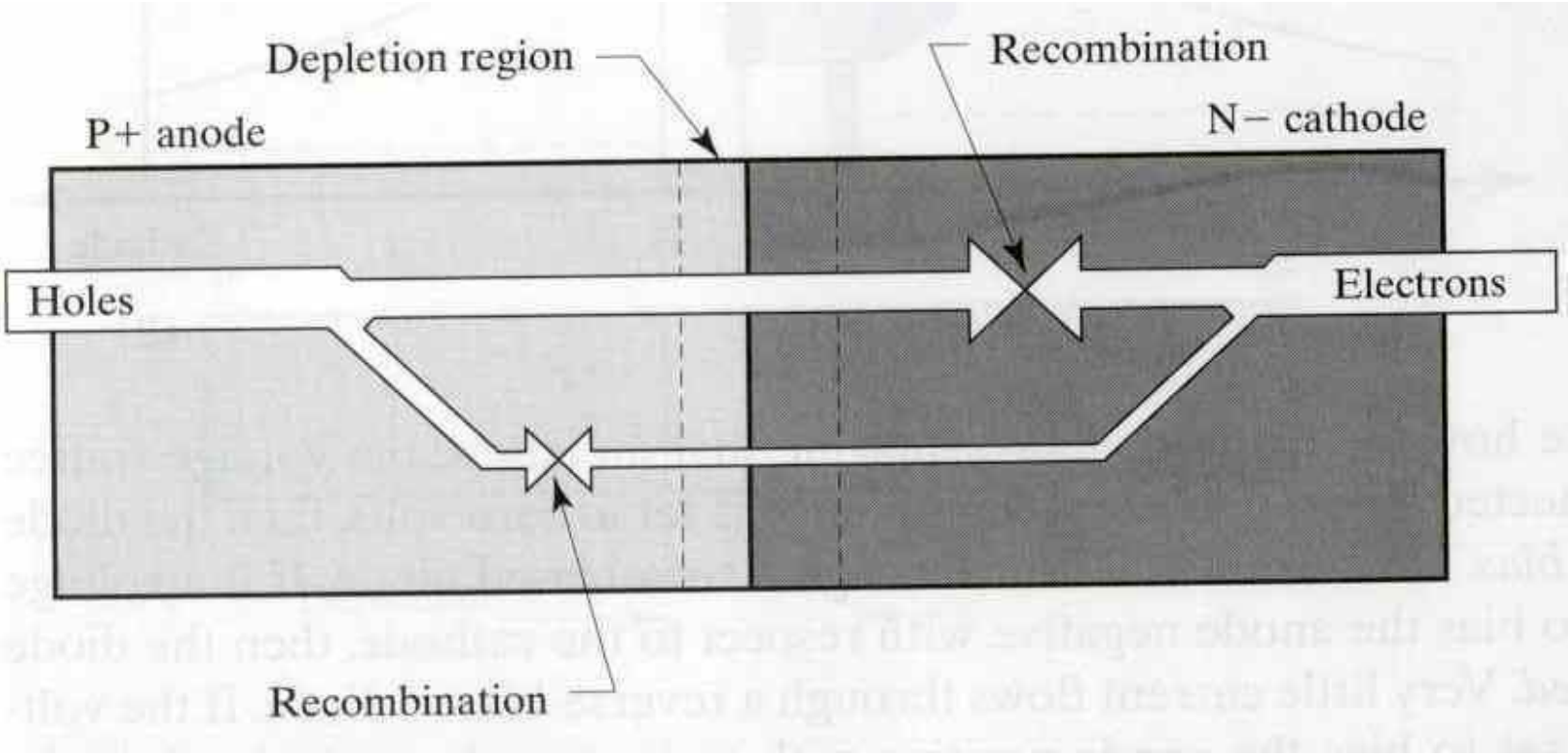
Typically avoided in Digital ICs !!

→ 大電流



http://hyperphysics.phy-astr.gsu.edu/Hbase/solids/diod.html

Forward Bias carrier flow

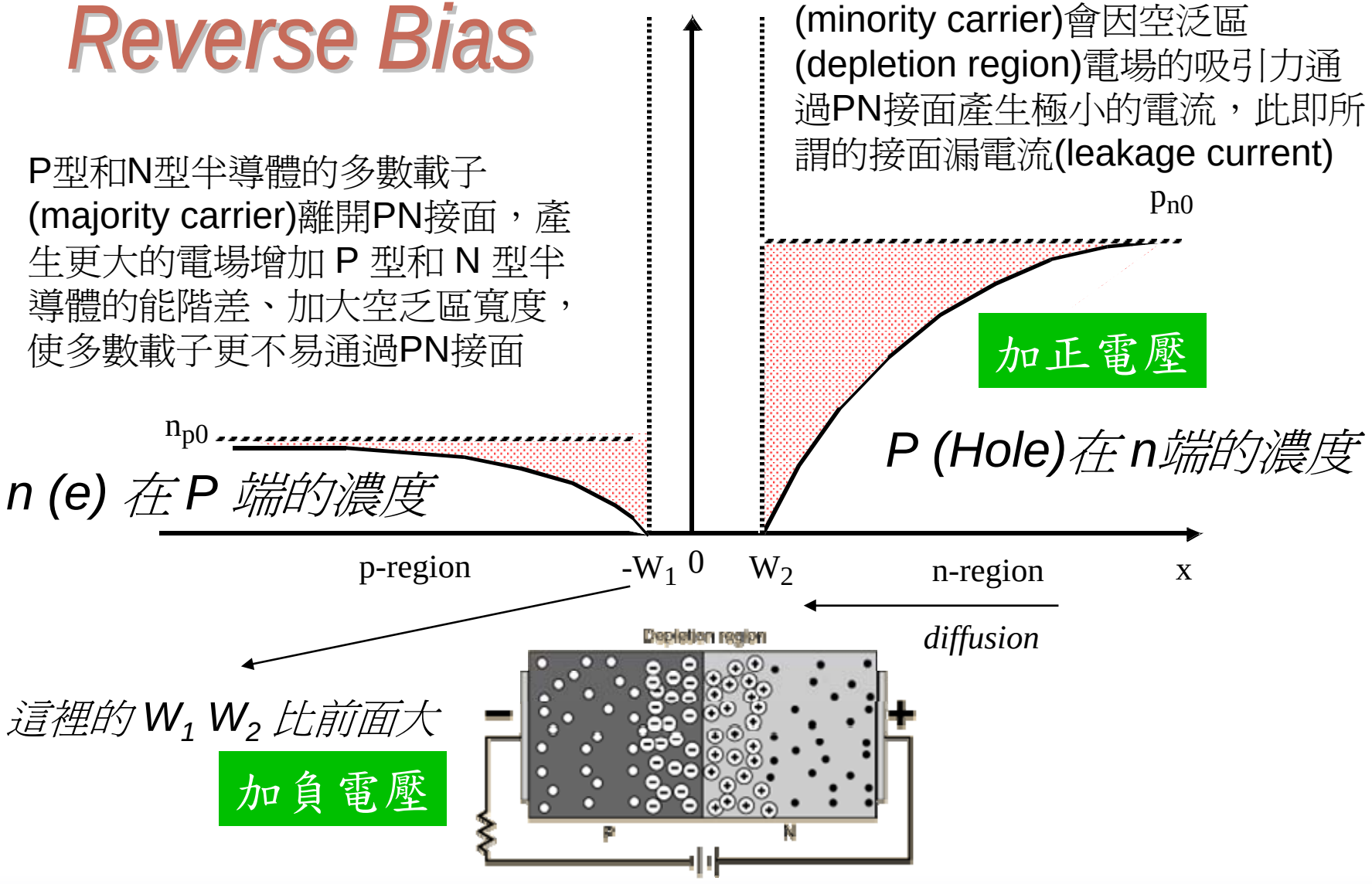


Carrier flow in a forward-biased PN Junction

Reverse Bias

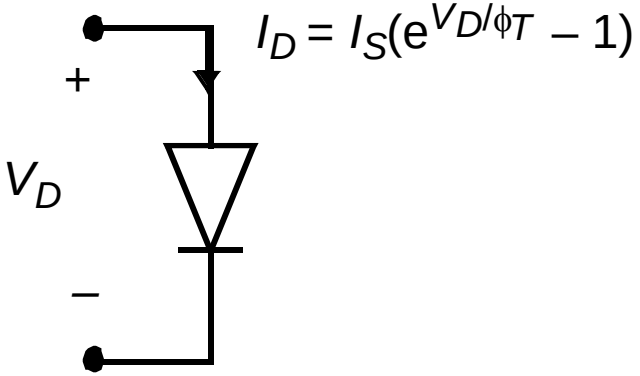
P型和N型半導體的多數載子(majority carrier)離開PN接面，產生更大的電場增加 P 型和 N 型半導體的能階差、加大空乏區寬度，使多數載子更不易通過PN接面

P型和N型半導體的少數載子(minority carrier)會因空泛區(depletion region)電場的吸引力通過PN接面產生極小的電流，此即所謂的接面漏電流(leakage current)

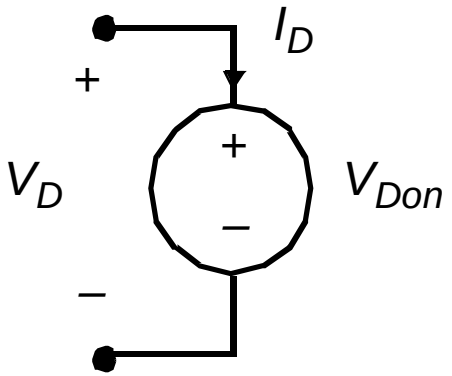


The Dominant Operation Mode

Models for Manual Analysis



(a) Ideal diode model

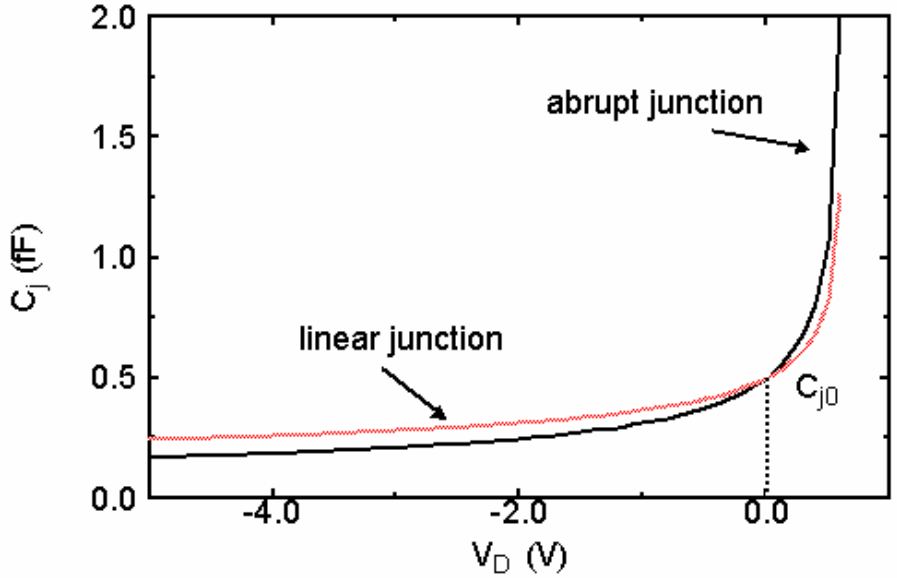


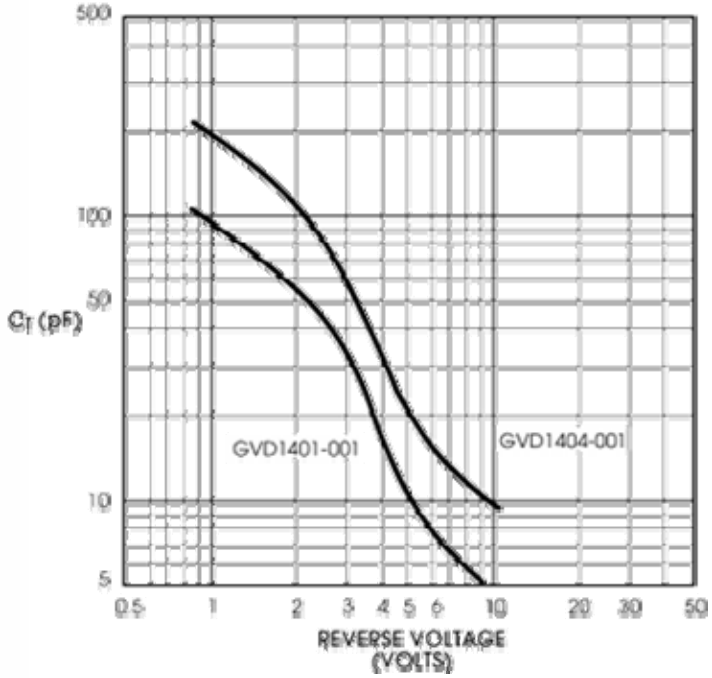
(b) First-order diode model

HW3-1

- Please describe the following terms
  - Forward Bias
  - Reverse Bias

Junction Capacitance





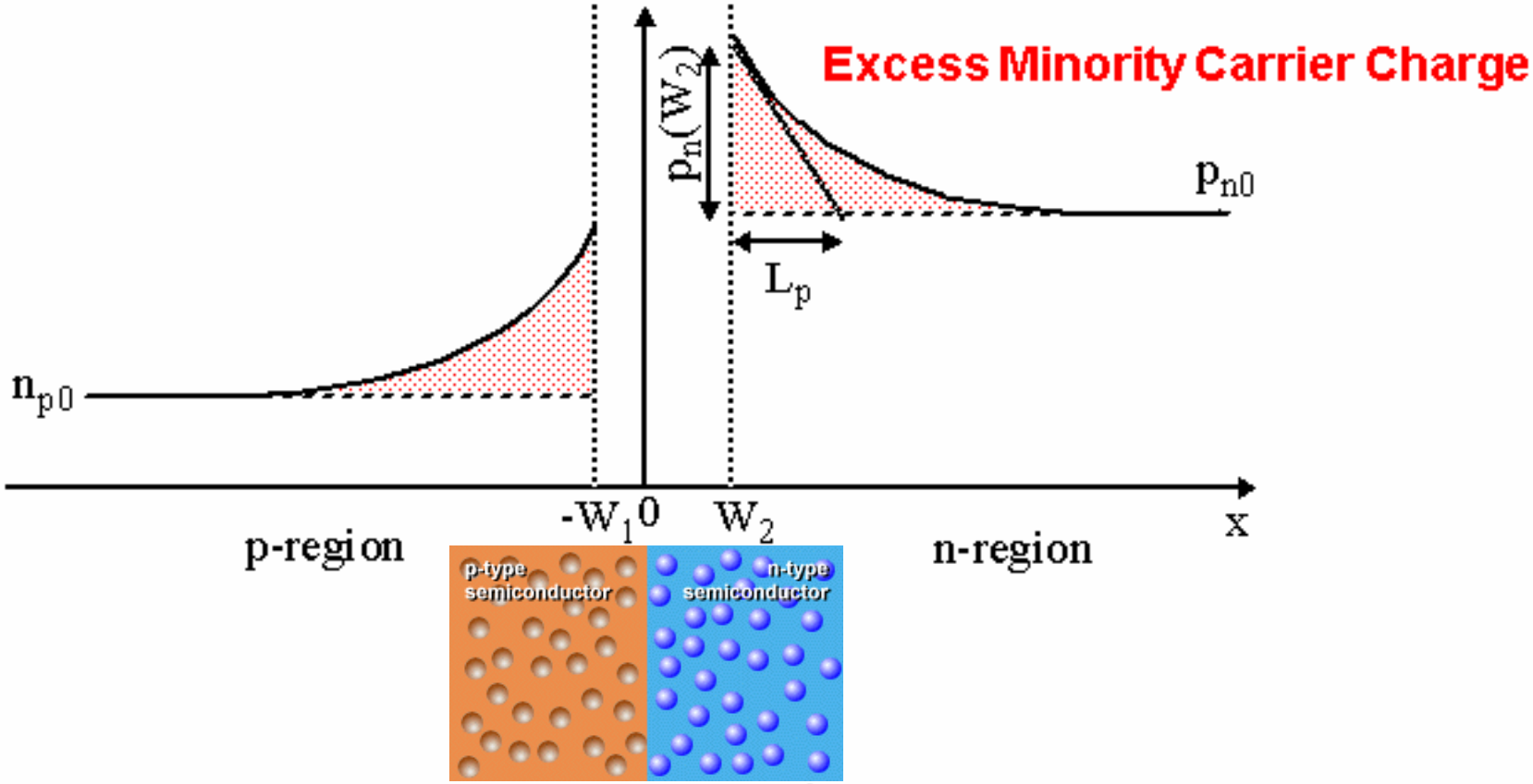
$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

m = 0.5: abrupt junction
m = 0.33: linear junction

Sprague-Goodman varactor diode
(變容二極體)

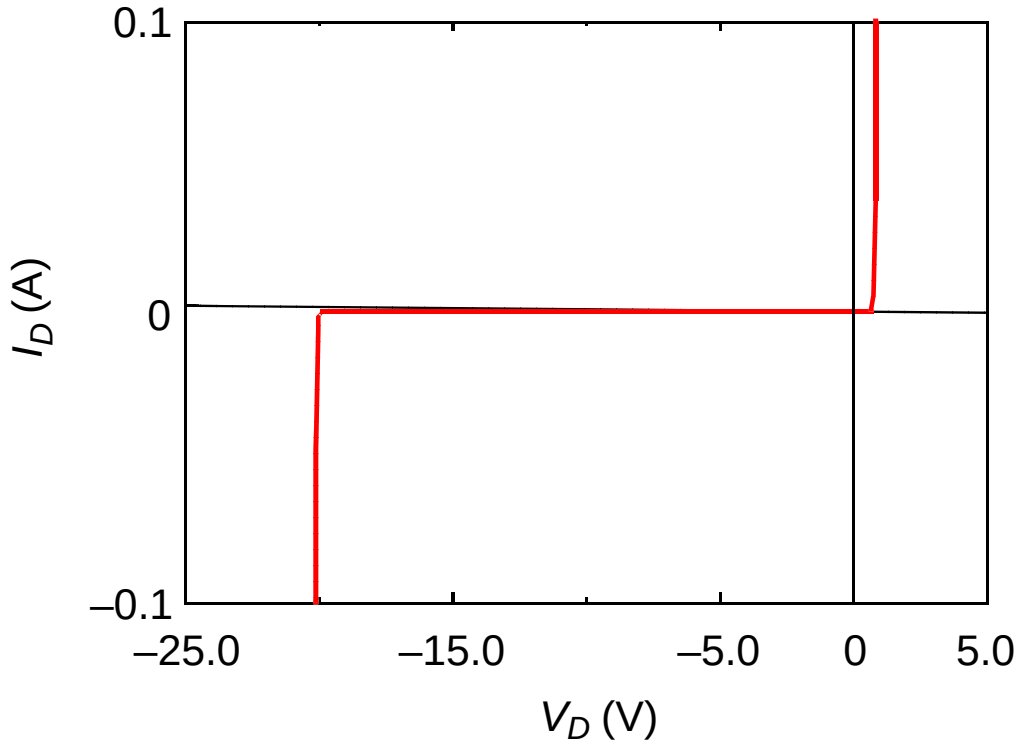
http://www.spraguegoodman.com/gvd/gvd1400.html

Diffusion Capacitance



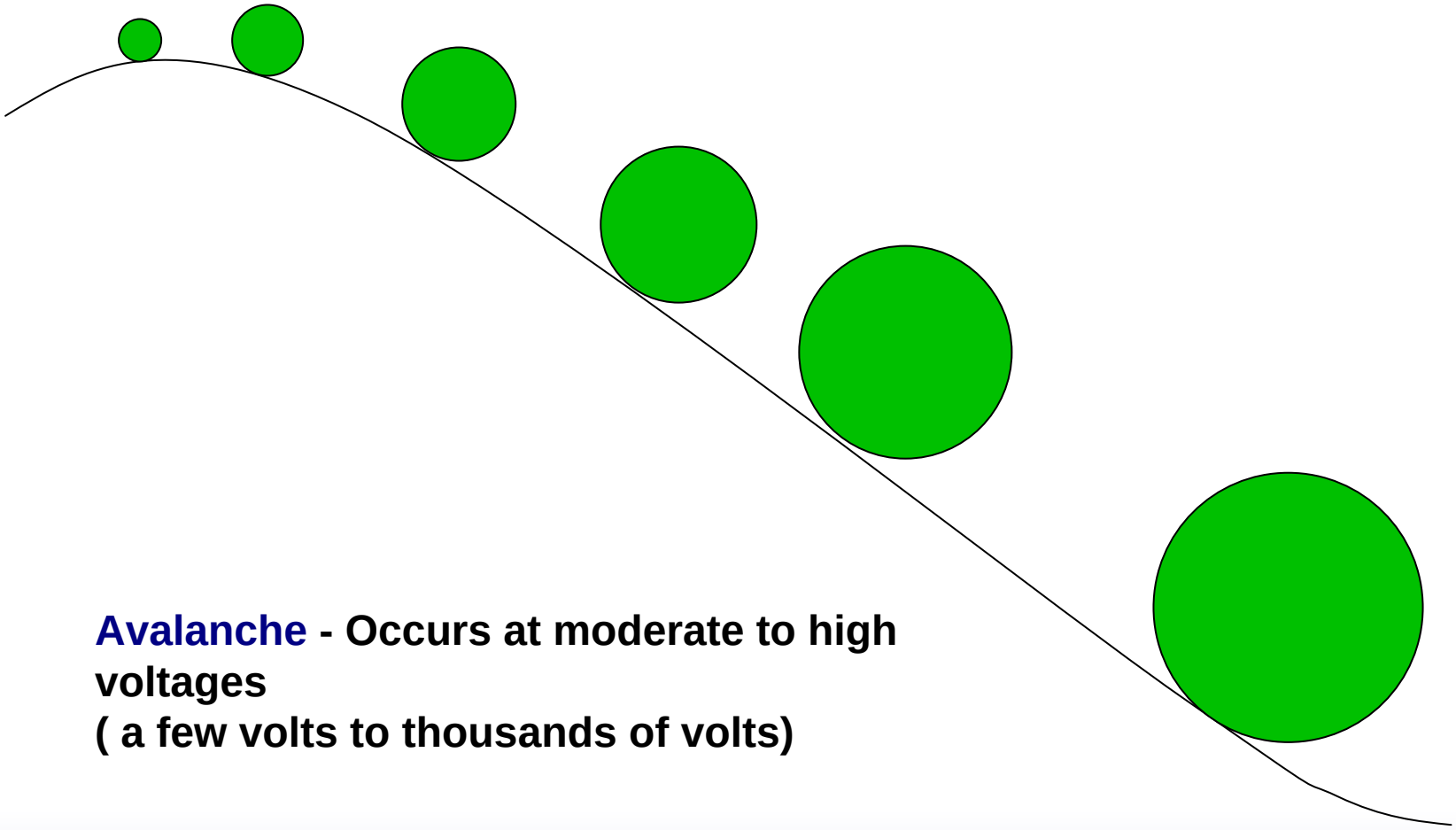
$$C_d = \frac{dQ_D}{dV_D} = \tau_T \frac{dI_D}{dV_D} \approx \frac{\tau_T I_D}{\phi_T}$$

Secondary Effects



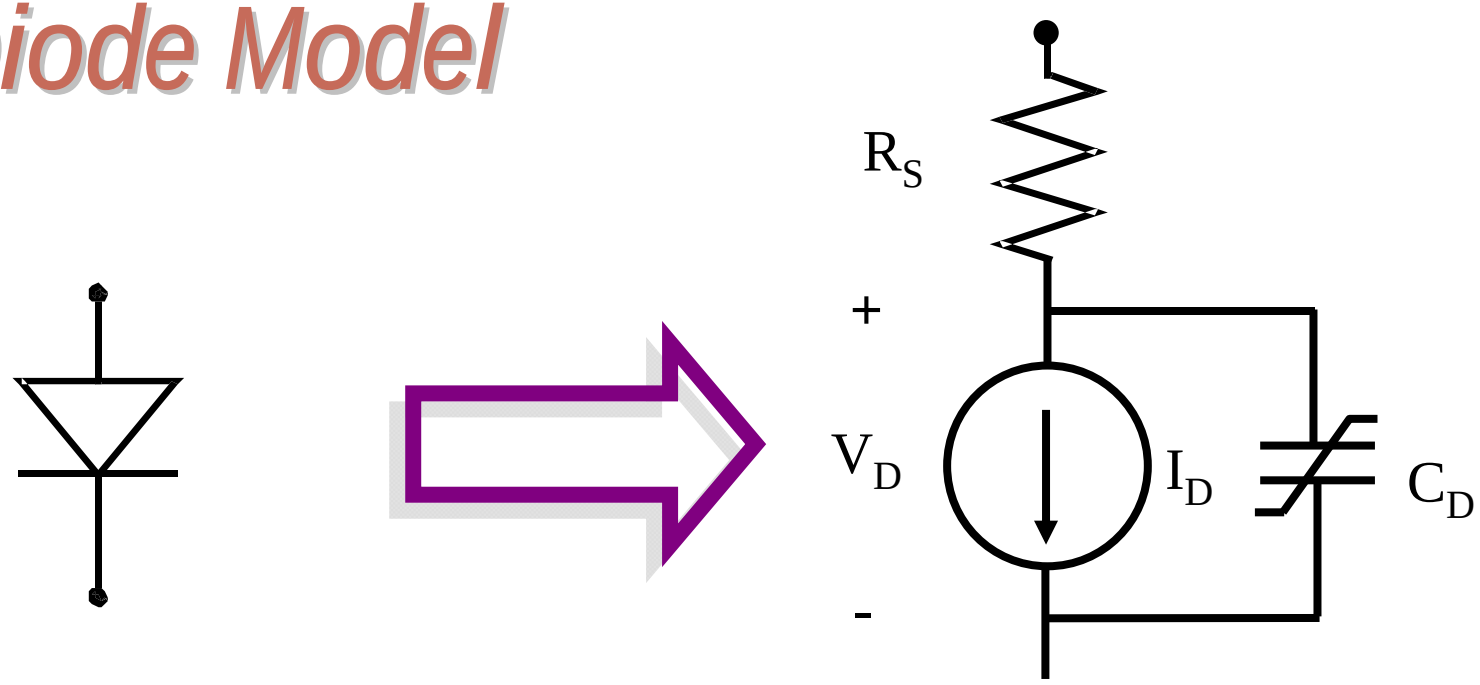
Avalanche Breakdown

Avalanche Breakdown

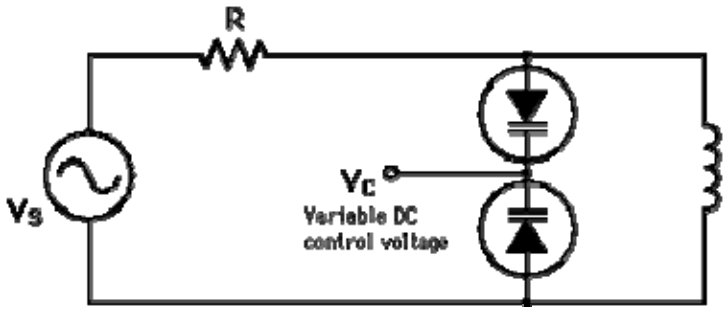


Avalanche - Occurs at moderate to high voltages
(a few volts to thousands of volts)

Diode Model

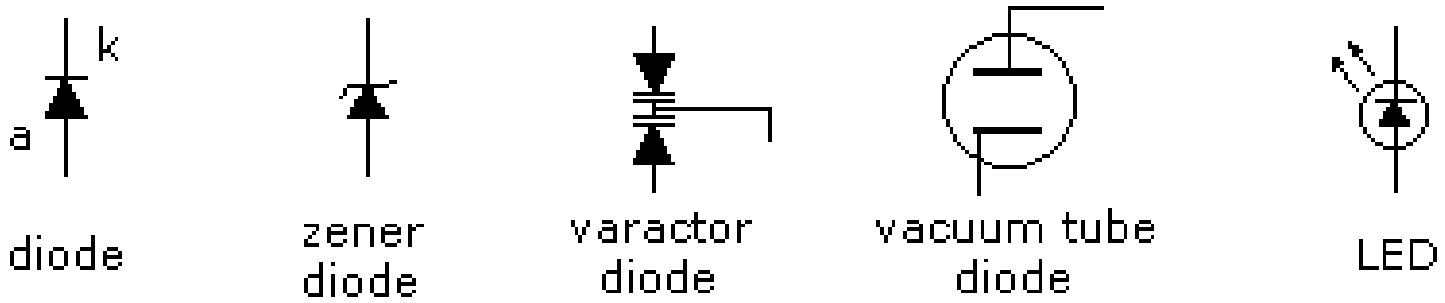


Application: Varactor Tuner



http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/varactor.html

Schematic Symbols for Diodes



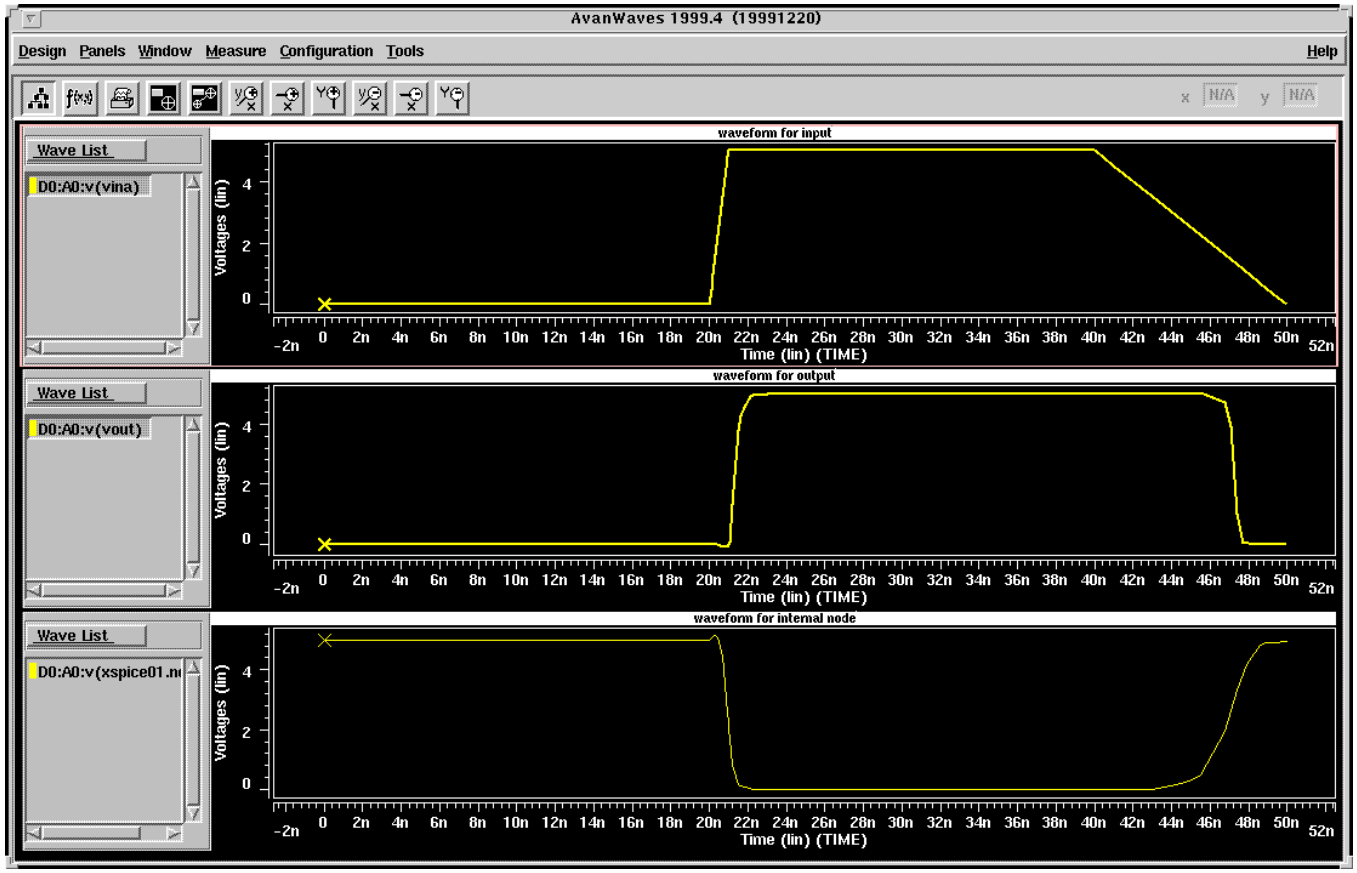
SPICE Parameters (Diode)

Parameter Name	Symbol	SPICE Name	Units	Default Value
Saturation current	I_S	IS	A	1.0 E-14
Emission coefficient	n	N	-	1
Series resistance	R_S	RS	Ω	0
Transit time	τ_T	TT	sec	0
Zero-bias junction capacitance	C_{j0}	CJ0	F	0
Grading coefficient	m	M	-	0.5
Junction potential	ϕ_0	VJ	V	1

First Order SPICE diode model parameters.

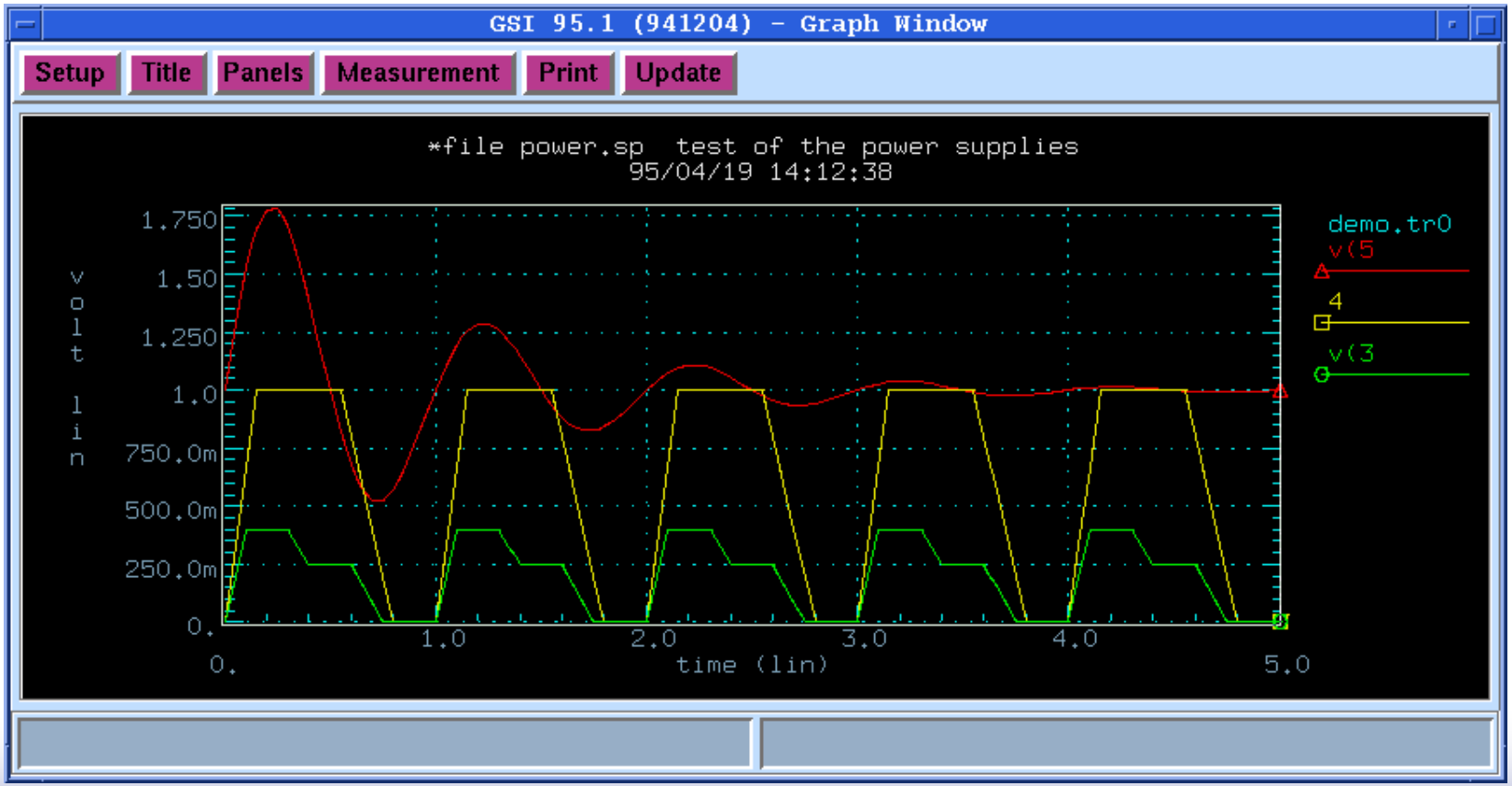
HSPICE (1/2)

- Digital or Analog ?



HSPICE (2/2)

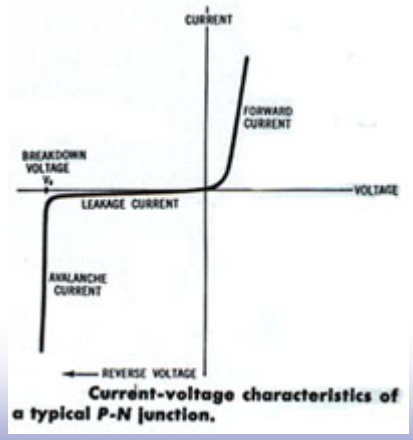
- Digital or Analog ?



HW3-2

- What are the applications of Diodes ?
  - Symbol
  - Function
  - Applications
  - Real products (Company and model names is needed)

Zener Diode

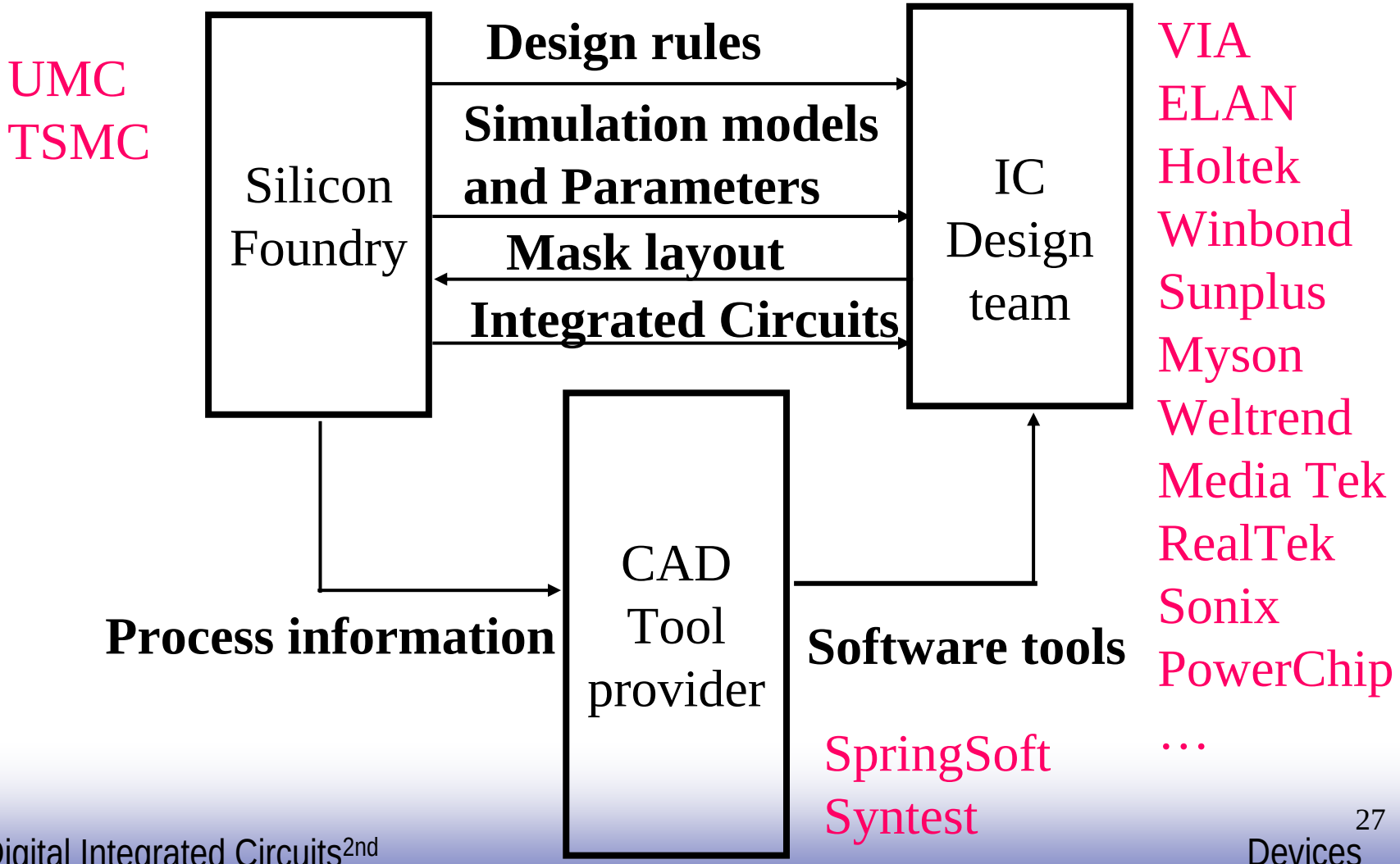


Current-voltage characteristics of a typical P-N junction.

FAIRCHILD SEMICONDUCTOR™

1N4722A

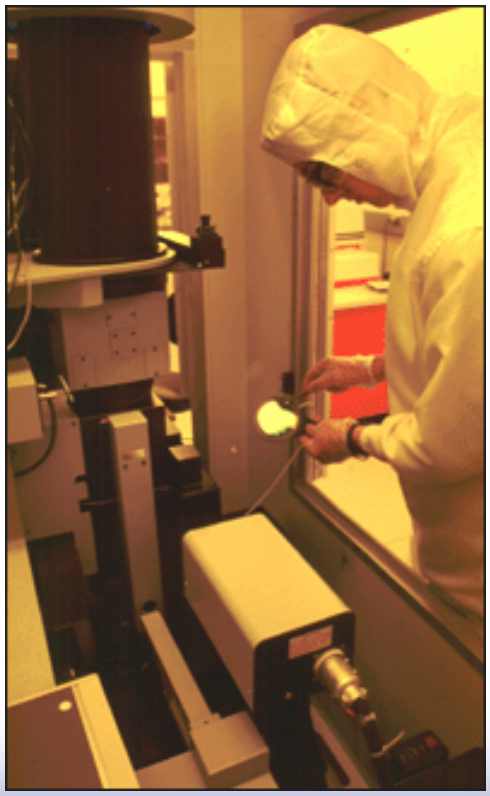
Relationship between a silicon foundry, and IC design team, and a CAD tool provider



IDM (Integrated Device Manufacturer)

- MOSEL
- SiS
- Winbond
- MXIC

- IBM
- LG
- TI



Design

Fabrication

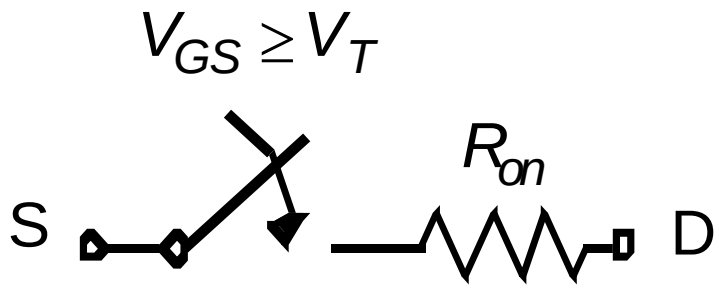
HW#3-3

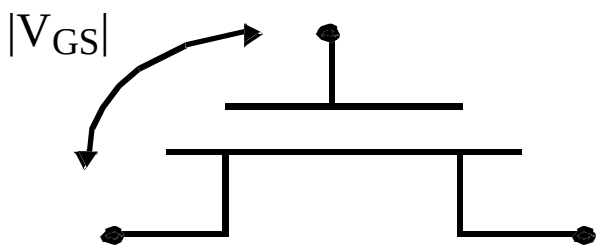
- IC Design Houses
  - Please find out the websites of 15 IC design houses in Taiwan stock market.
  - Please write down their English and Chinese names.
  - Please find out the logo of each company.

台灣積體電路 **TSMC (Taiwan Semiconductor Manufacture Company)**
www.tsmc.com

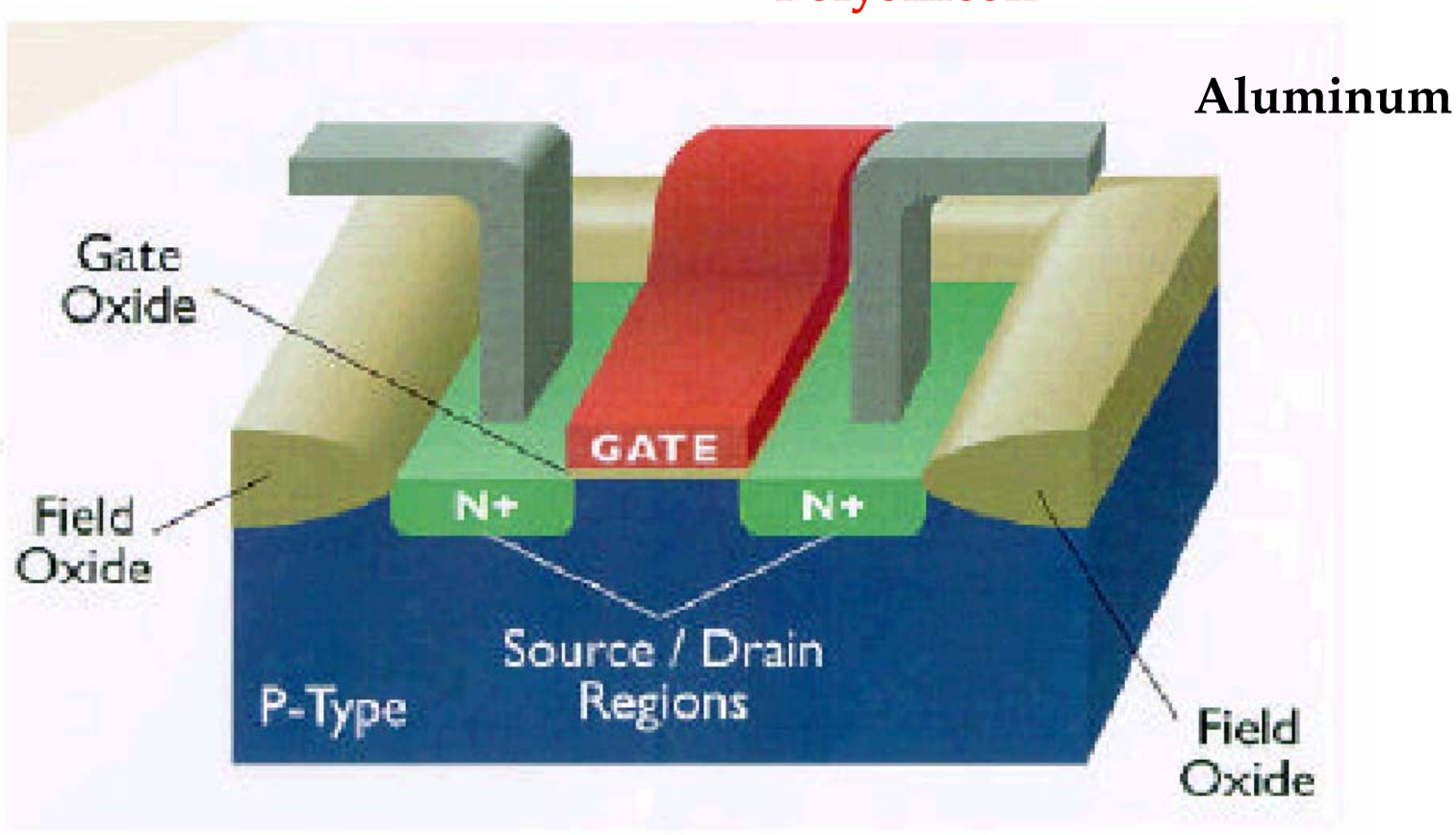
What is a Transistor?

A Switch! ⟷ An MOS Transistor

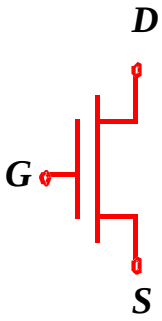




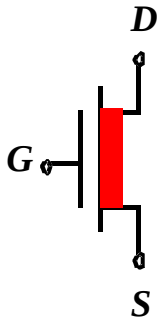
The MOS Transistor



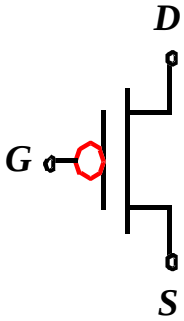
MOS Transistors - Types and Symbols



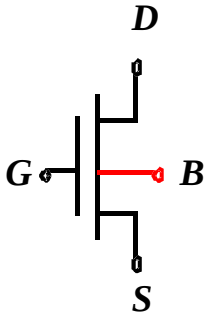
NMOS **Enhancement**



NMOS **Depletion**

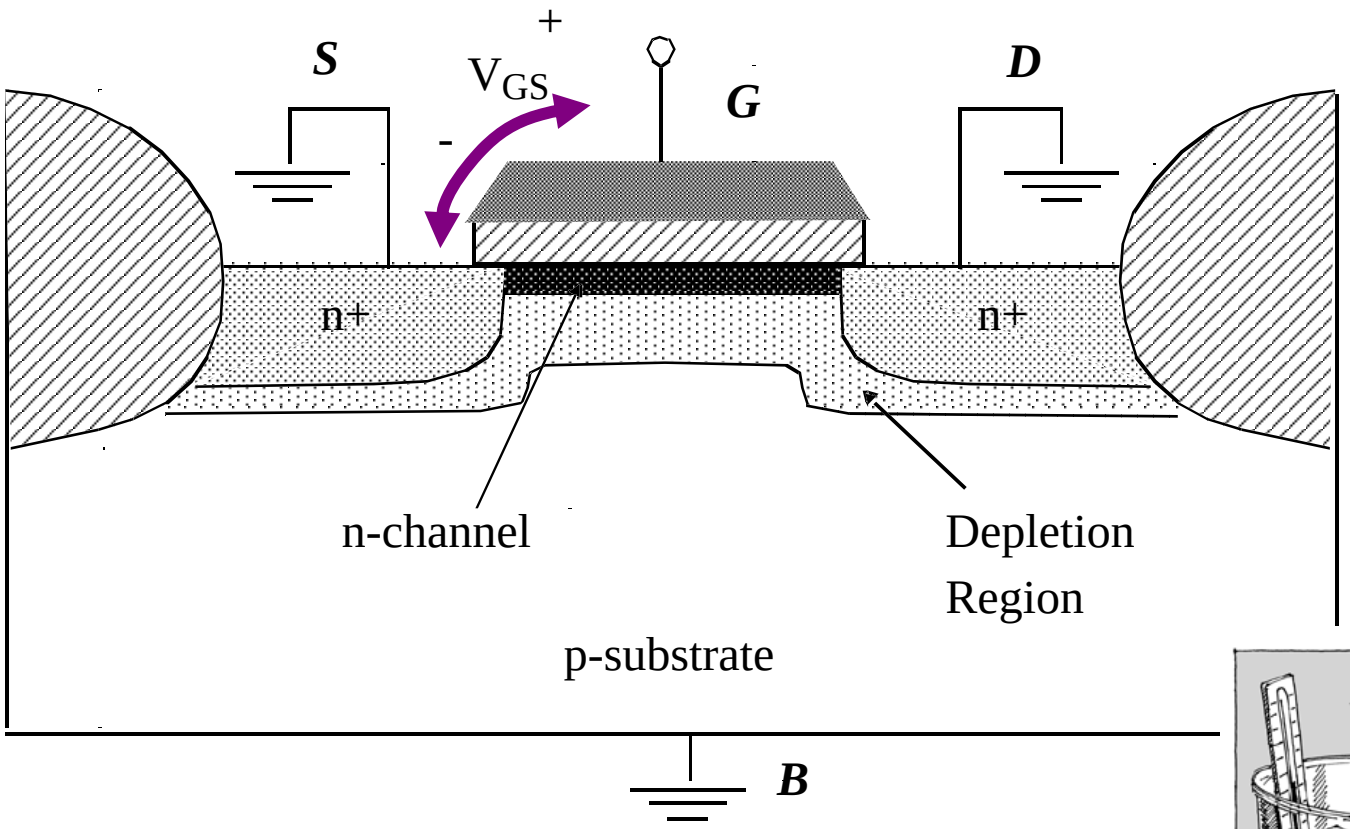


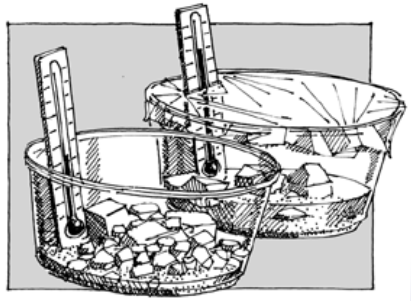
PMOS **Enhancement**



NMOS with **Bulk Contact**

Threshold Voltage: Concept



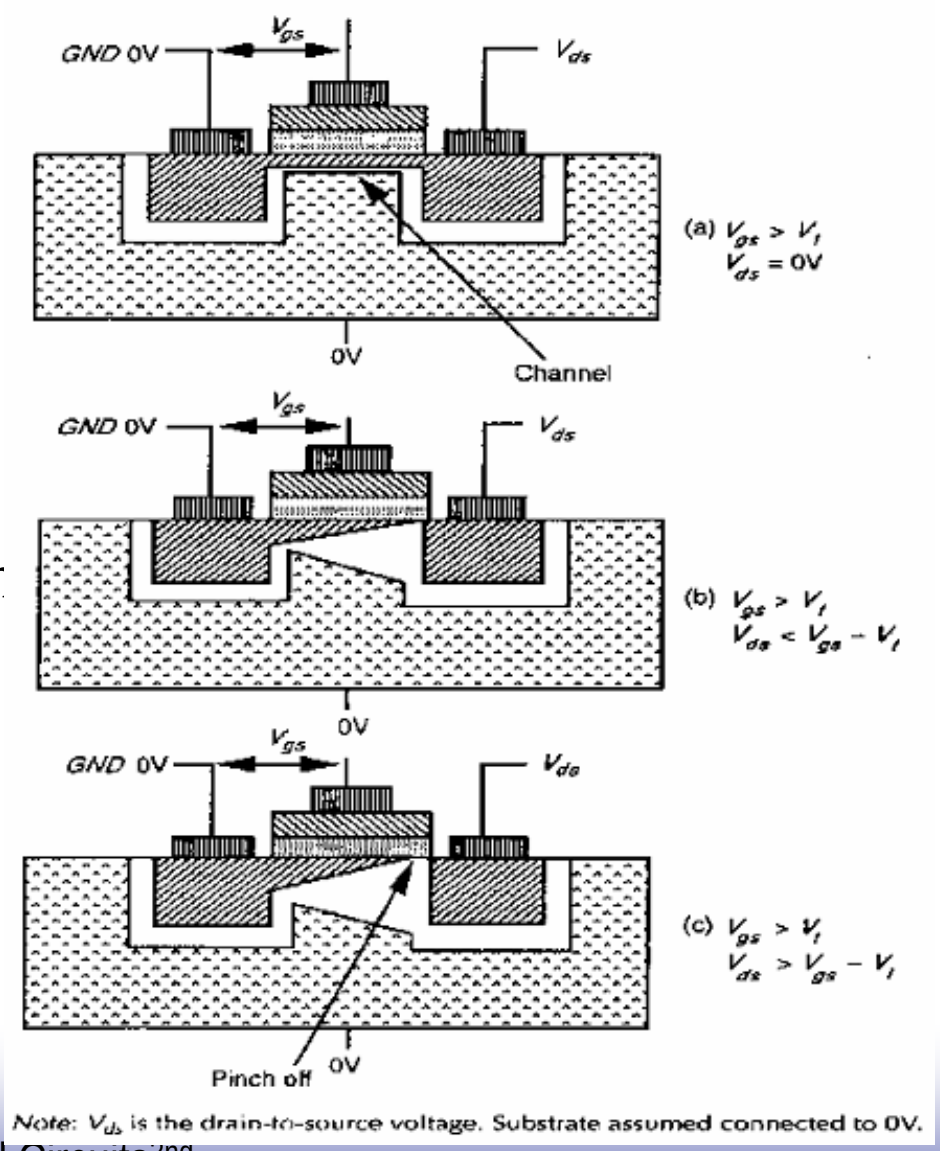


Operation Regions of a MOS Transistor

Cut off

Linear regior

Saturation



The Threshold Voltage V_T

$$V_T = \phi_{ms} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

Workfunction Difference

Depletion Layer Charge

Surface Charge

Implants

Body Effect Coefficient

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

with

$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

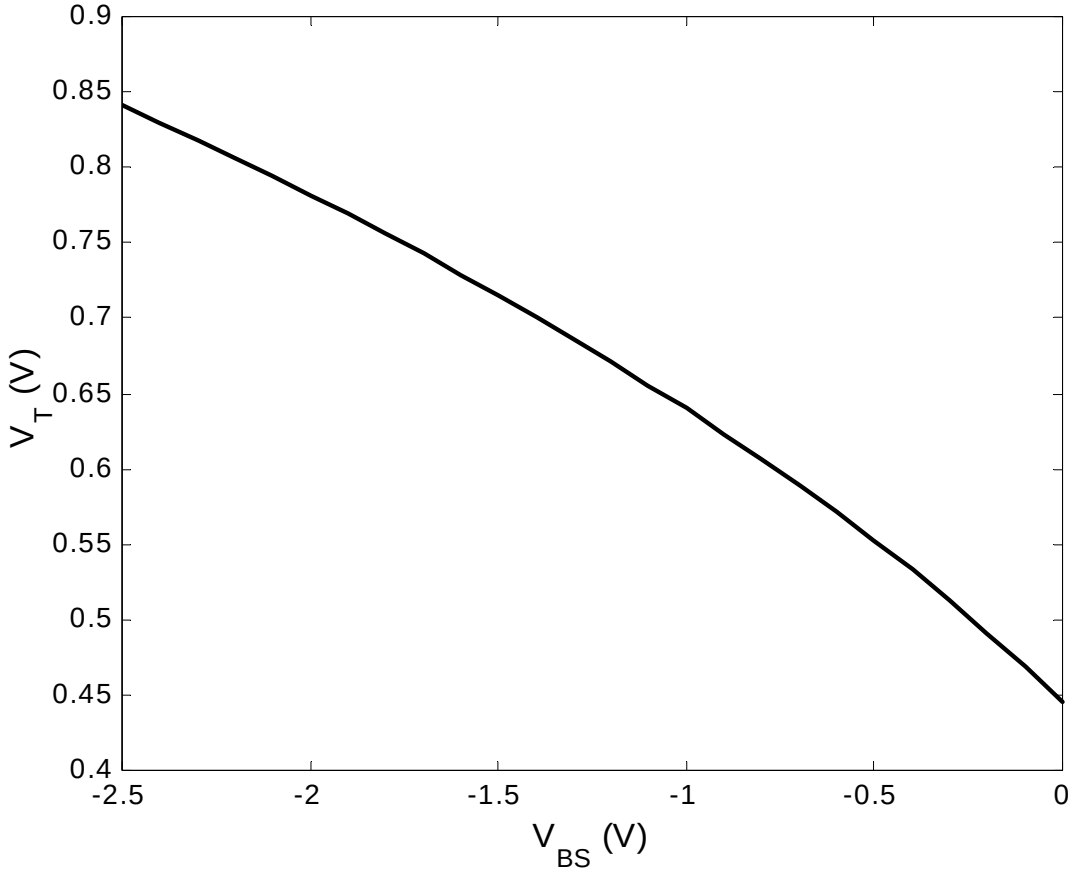
and

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

- V= Q/C
- C = ε * A/d
  - 所以 若 oxide 厚度 ↑
  - C_{ox} ↑
  - V ↓
  - V_T ↑
- V_{SB} ↑
  - V_T ↑

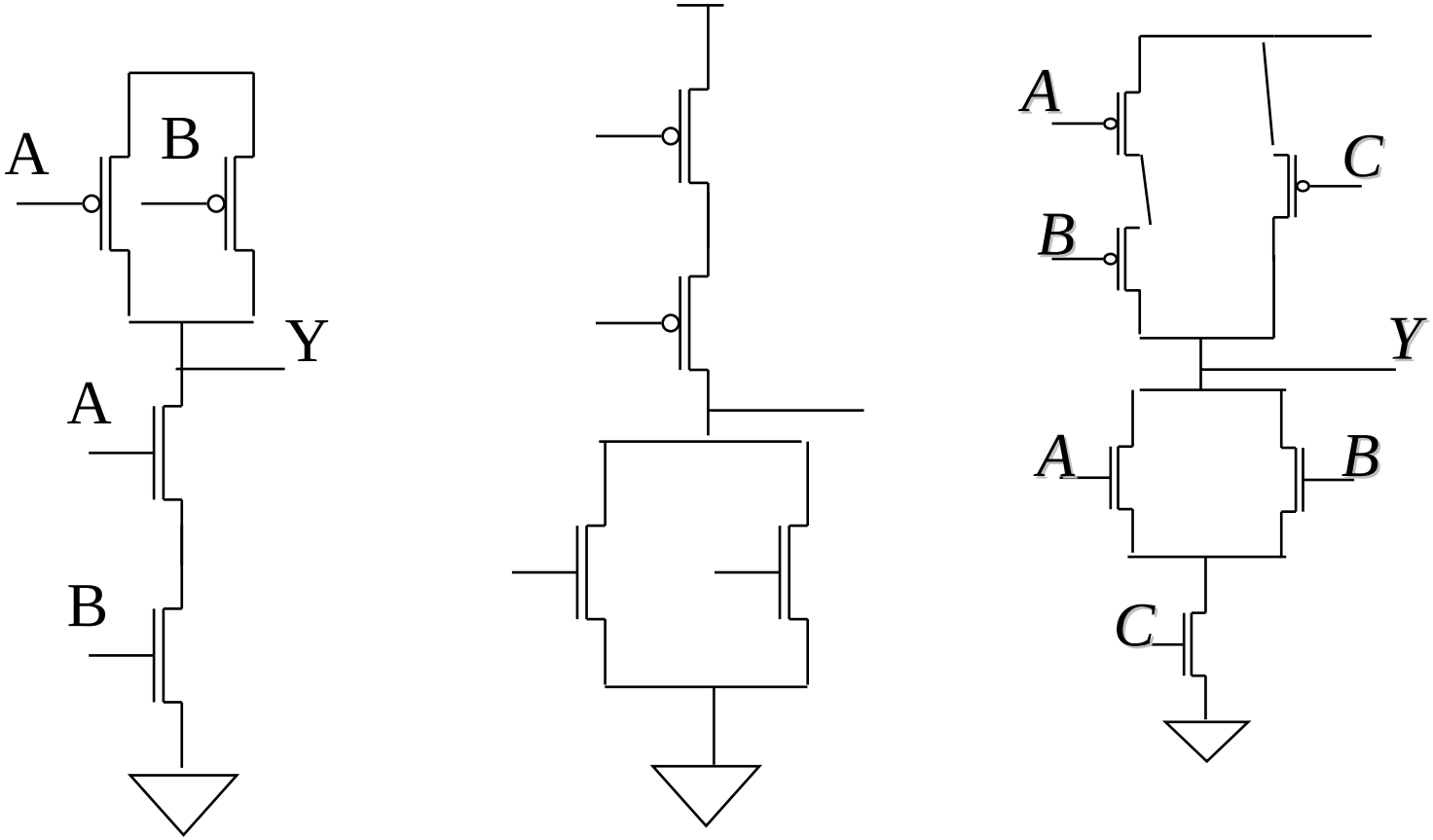
V_{T0} = Threshold voltage for V_{SB}=0

The Body Effect



Basic CMOS gates

- 2NAND 2NOR $\overline{AB+C}$

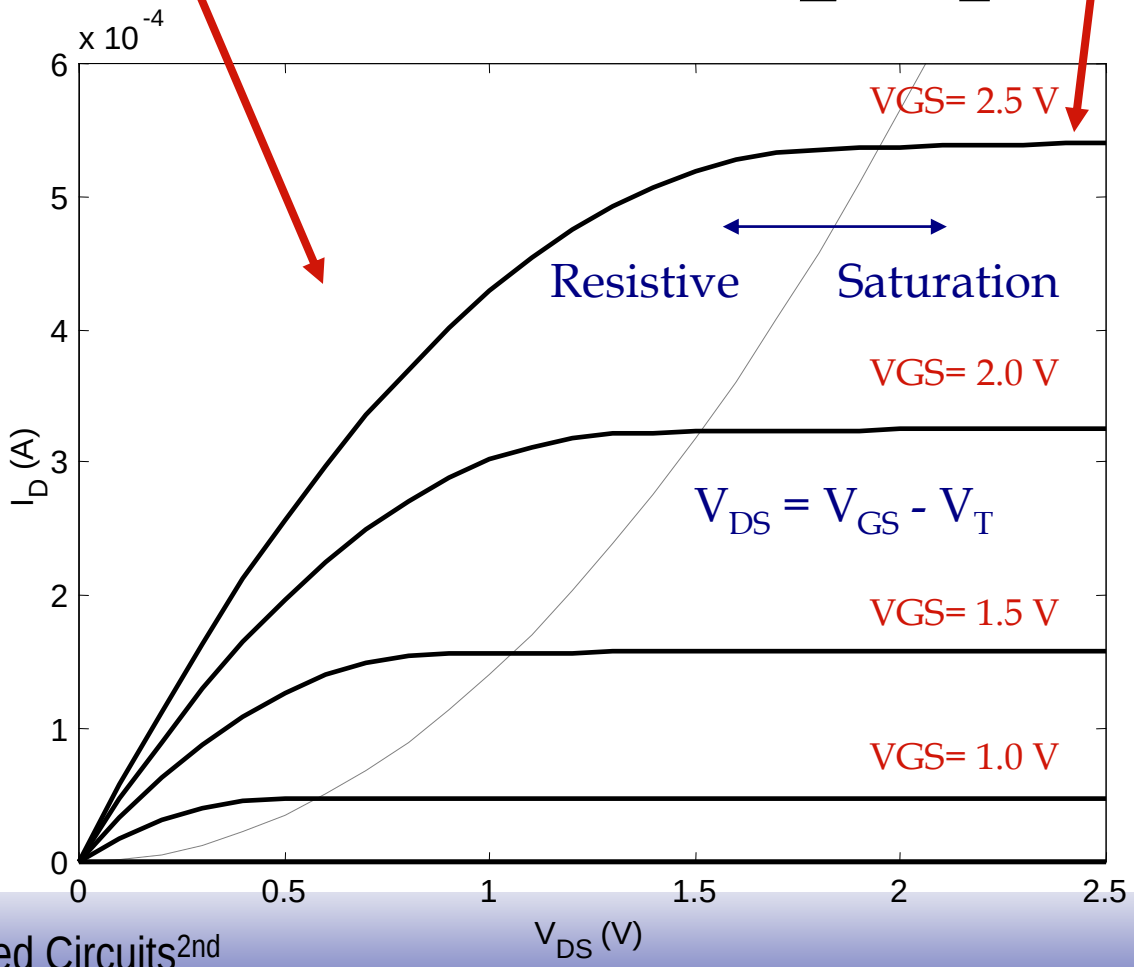


I-V Relations: A good ol' transistor

Old

$$I_{ds} = K\frac{W}{L}\left((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right)$$

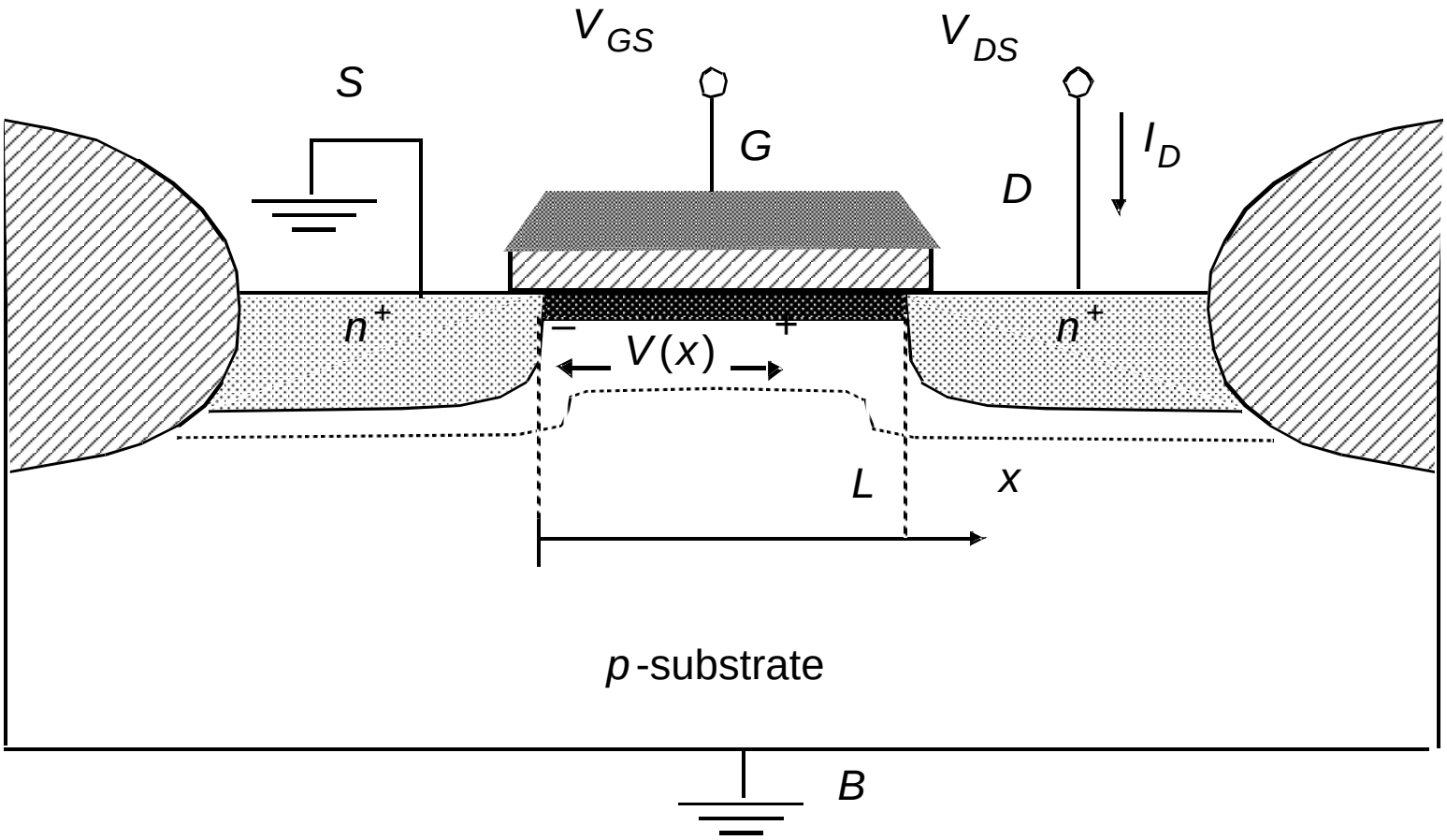
$$I_{ds} = K\frac{W}{L}\frac{(V_{gs} - V_t)^2}{2} = \frac{\beta}{2}(V_{gs} - V_t)^2$$



Quadratic Relationship

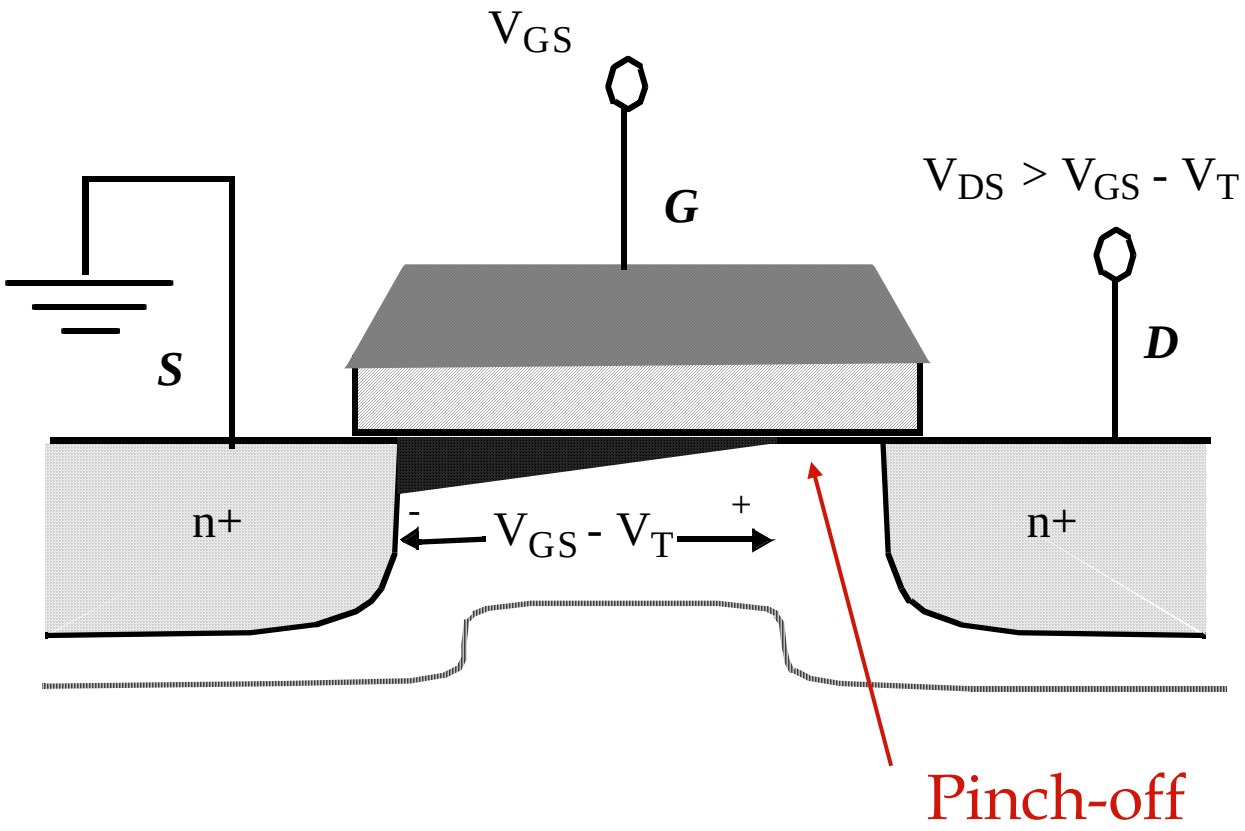
電流與 V_{gs} 平方成正比

Transistor in Linear Region



MOS transistor and its bias conditions

Transistor in Saturation Region



I-V Relations: Long-Channel Device

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

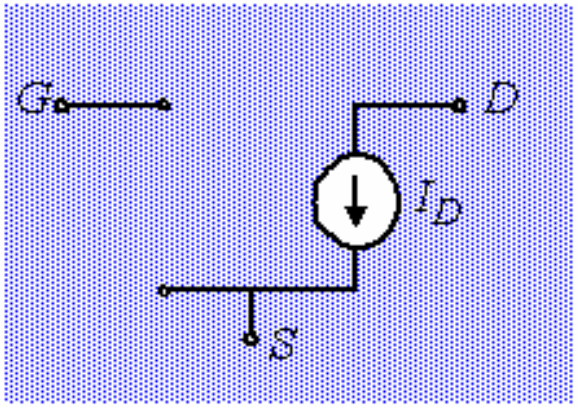
Process Transconductance Parameter

Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

A model for manual analysis



$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

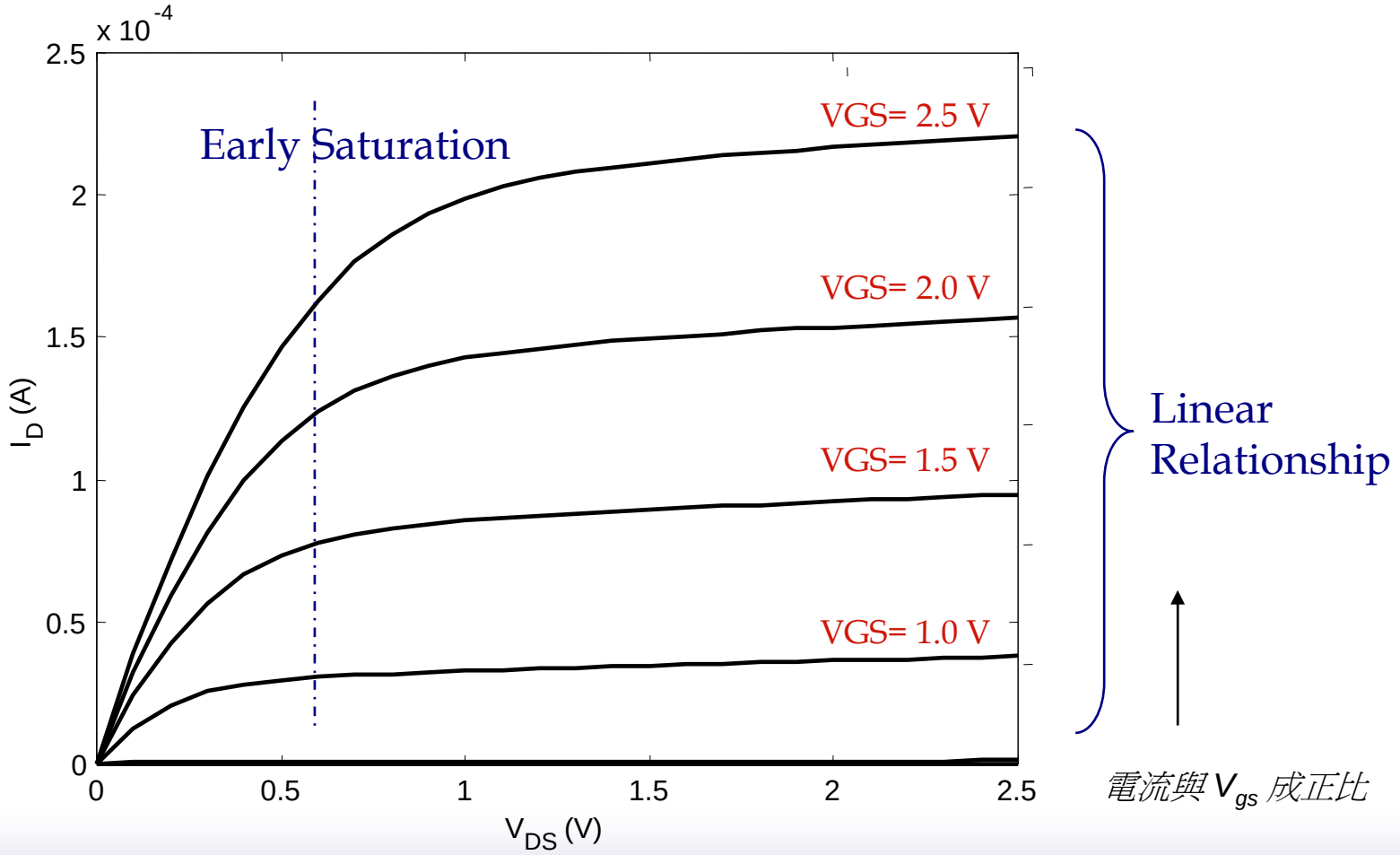
$$V_{DS} < V_{GS} - V_T$$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

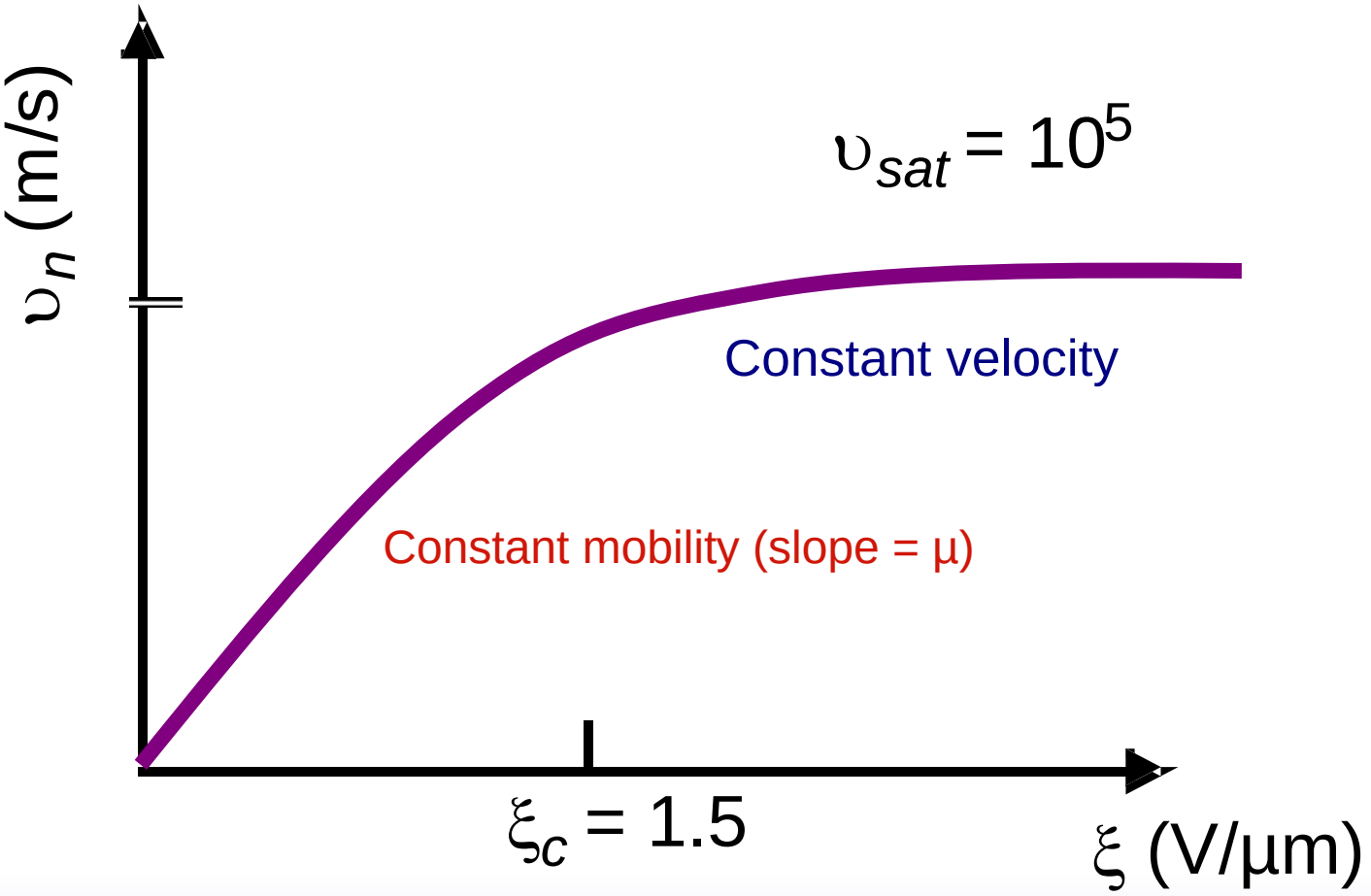
with

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|-2\phi_F\right|}\right)$$

Current-Voltage Relations
The Deep-Submicron Era

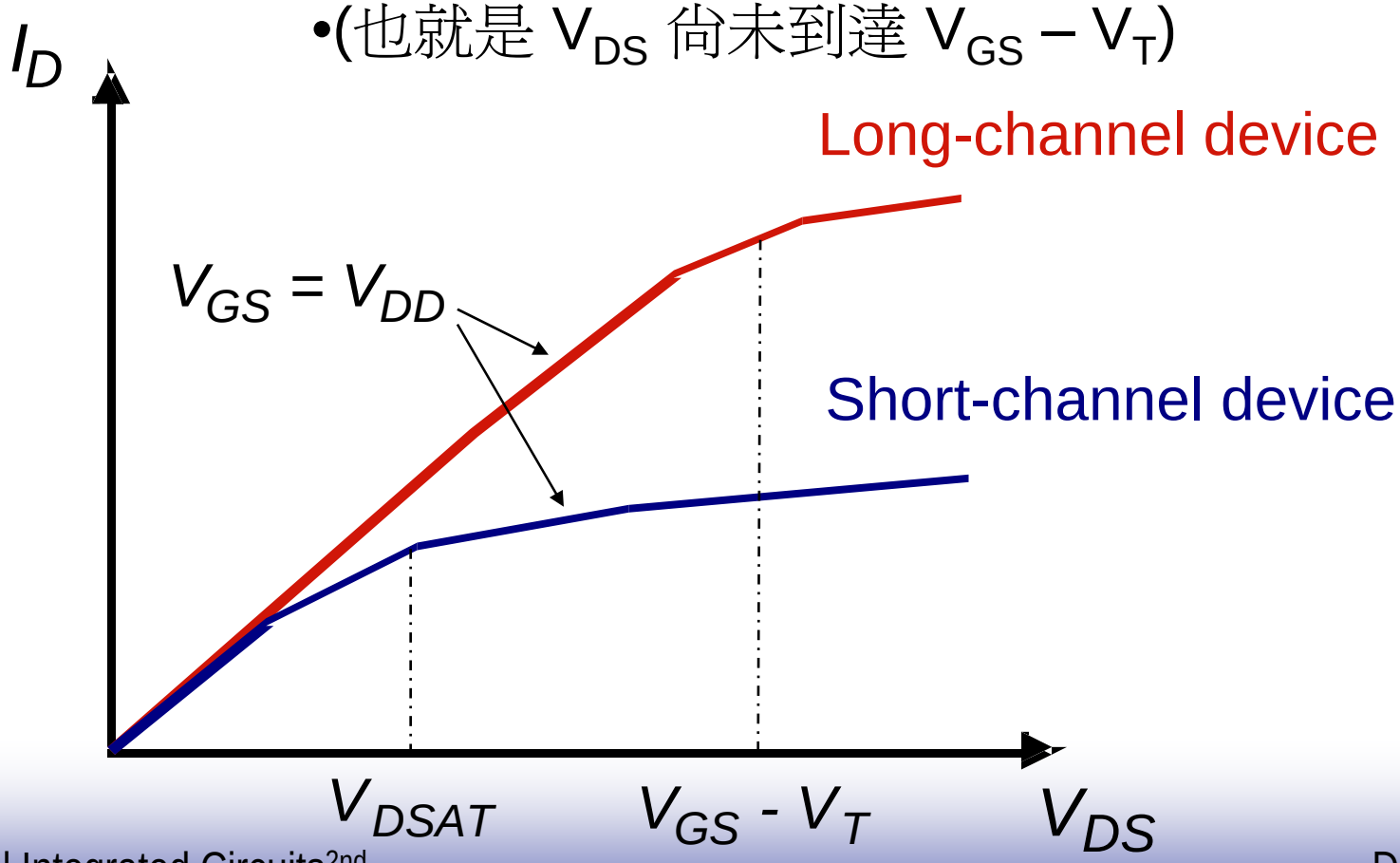


Velocity Saturation



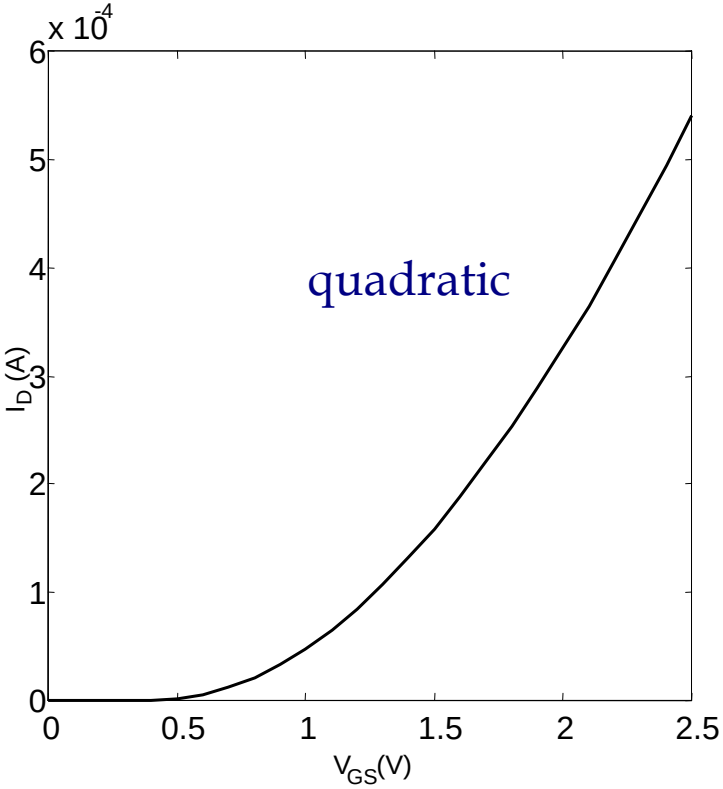
Long Channel vs. Short Channel (1/3)

- $V_{GT} = V_G - V_T$
- $V_{DSAT} = k\,(V_{GT})\,V_{GT}$
- *Short Channel k (VGT) < 1, 提早進入 Saturation,*
- (也就是 V_{DS} 尚未到達 $V_{GS} - V_T$)

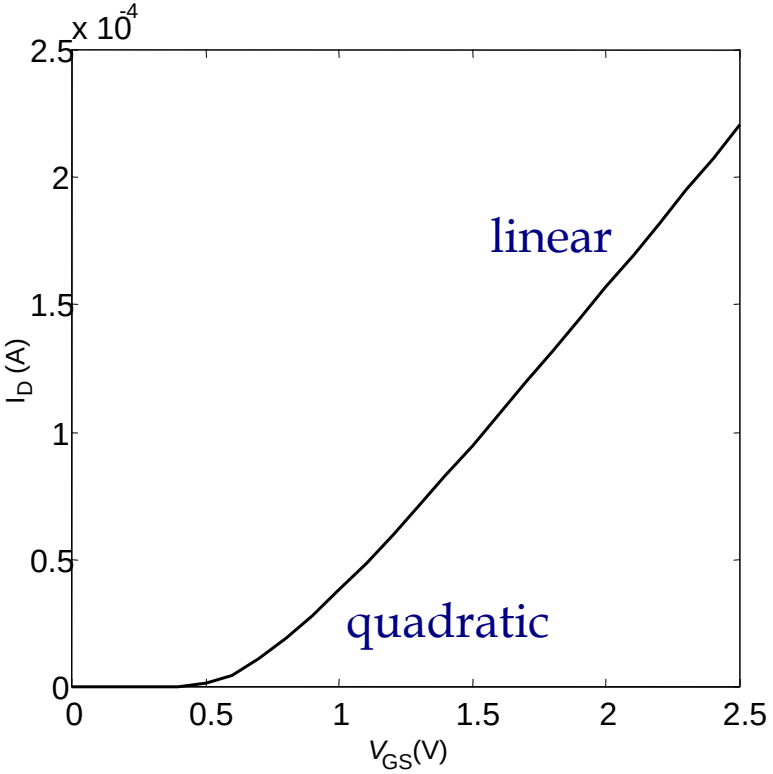


Long Channel vs. Short Channel (3/3)

I_D versus V_{GS}



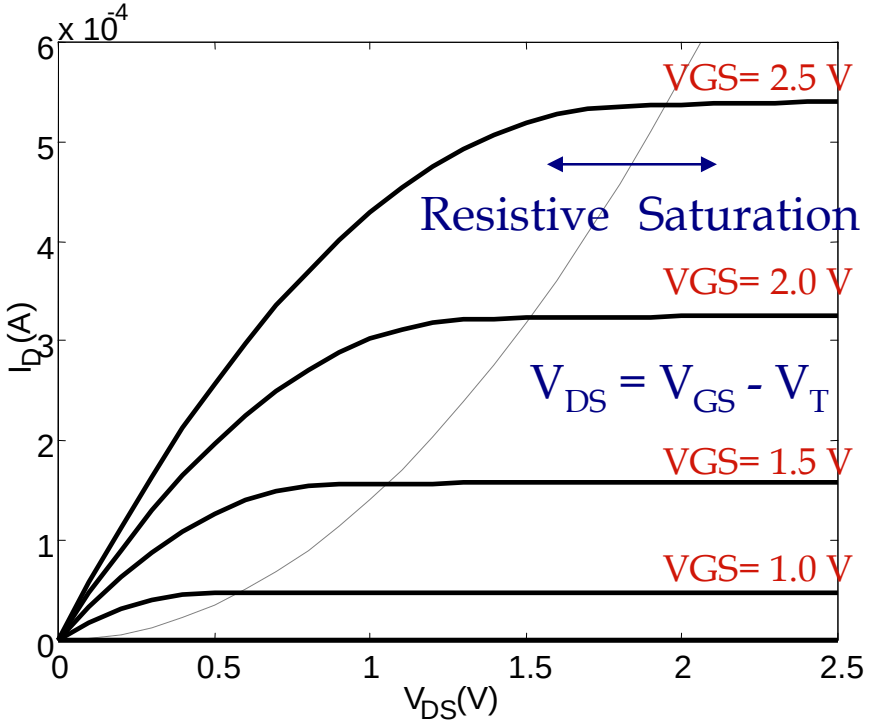
Long Channel



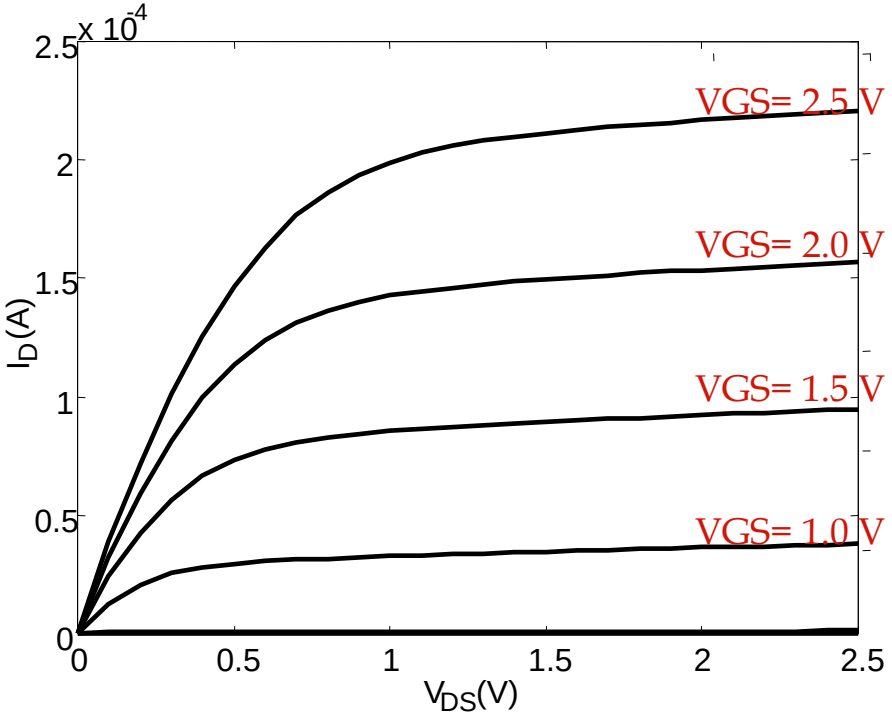
Short Channel

Long Channel vs. Short Channel (3/3)

I_D versus V_{DS}

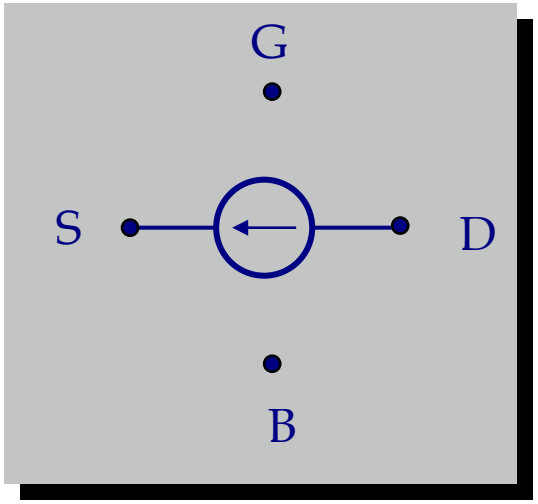


Long Channel



Short Channel

A unified model for manual analysis



$$I_D = 0 \text{ for } V_{GT} \le 0$$

$$I_D = k' \frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

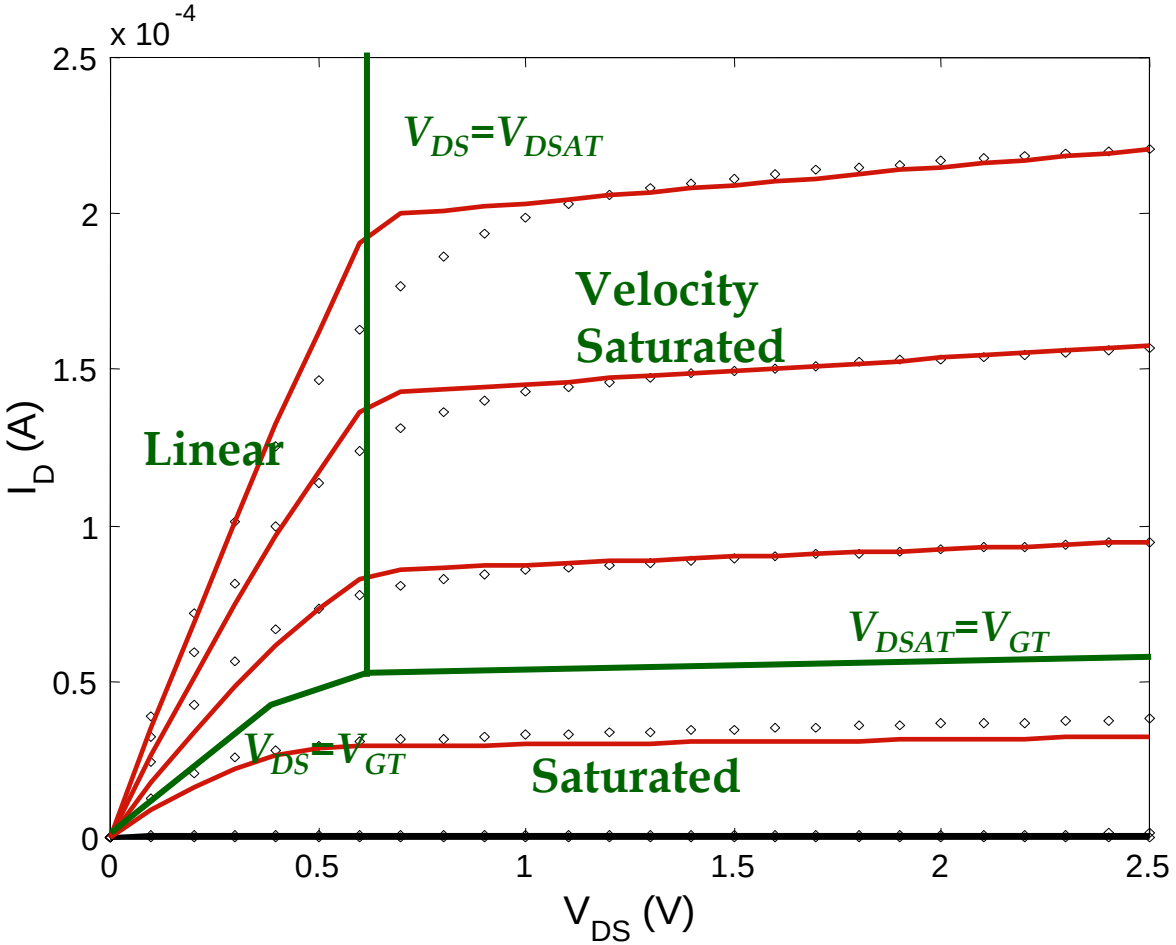
with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

$V_{GT} = V_{GS} - V_T$,

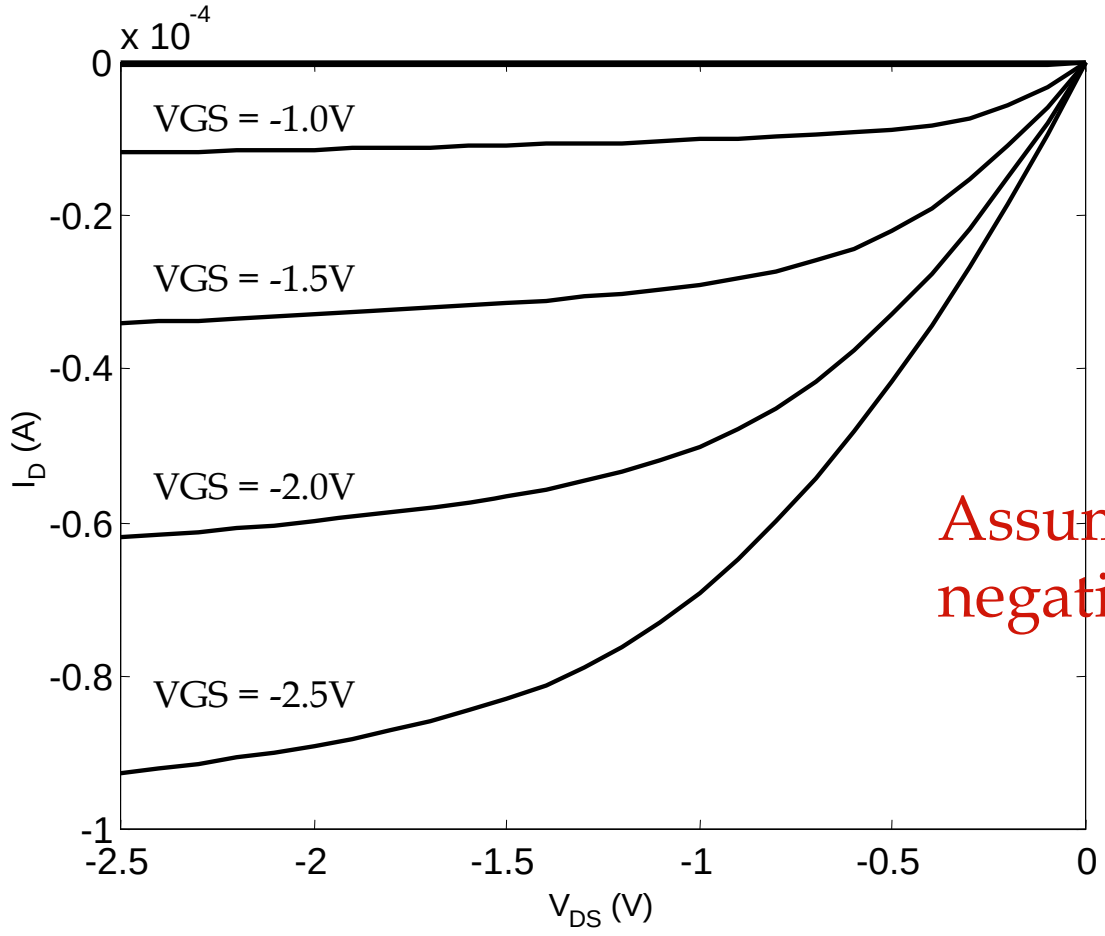
and $V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$

Skip…

Simple Model versus SPICE



A PMOS Transistor



Assume all variables negative!

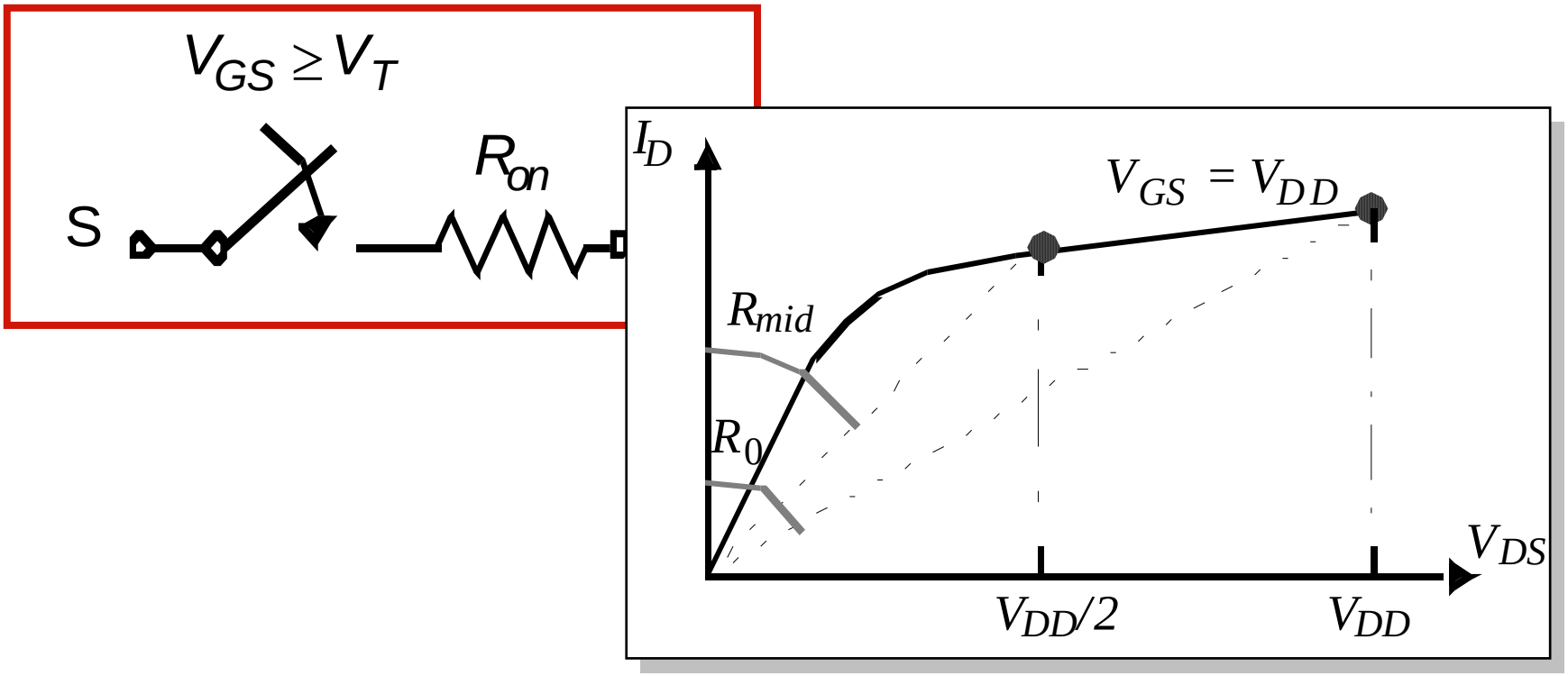
Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	K' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

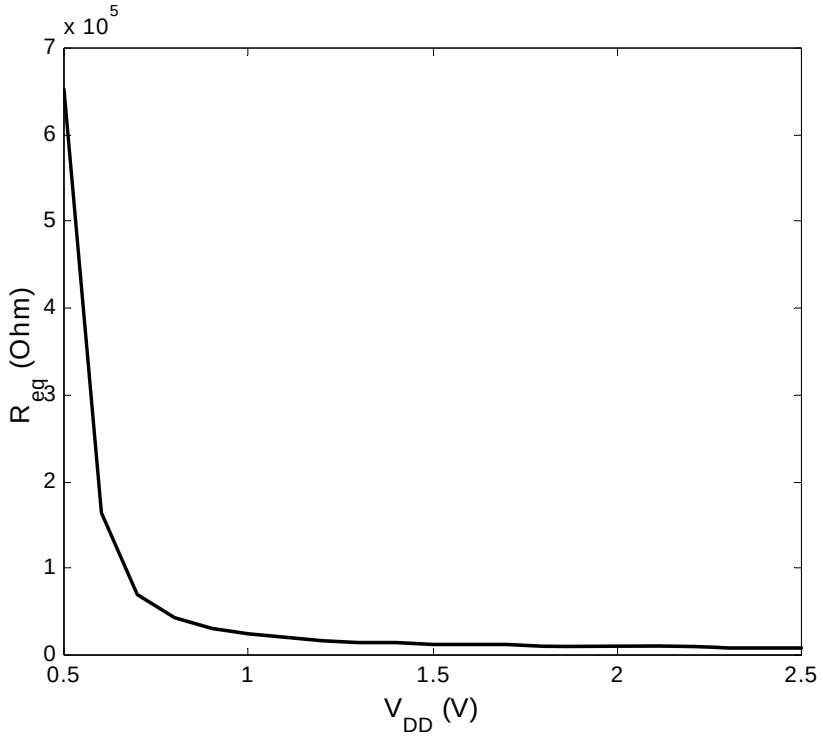
The Transistor as a Switch

MOS 是一個理想的開關嗎 ？



$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{5}{6}\lambda V_{DD}\right)$$

The Transistor as a Switch



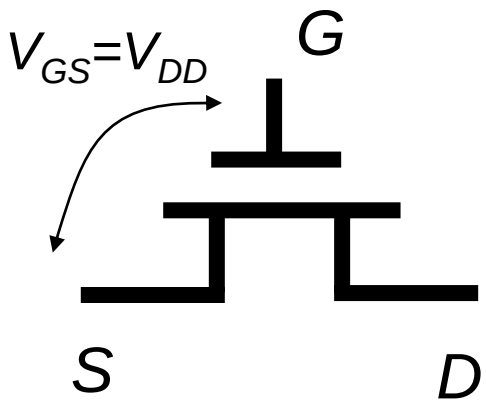


Fig. 3.28 Simulated equivalent resistance of a minimum size NMOS transistor in 0.25um CMOS process as function of V_{DD} ($V_{GS}=V_{DD}$, $V_{DS}=V_{DD}$) → $V_{DD}/2$

The Transistor as a Switch

Table 3.3 Equivalent resistance R_{eq} (W/L= 1) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L.

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

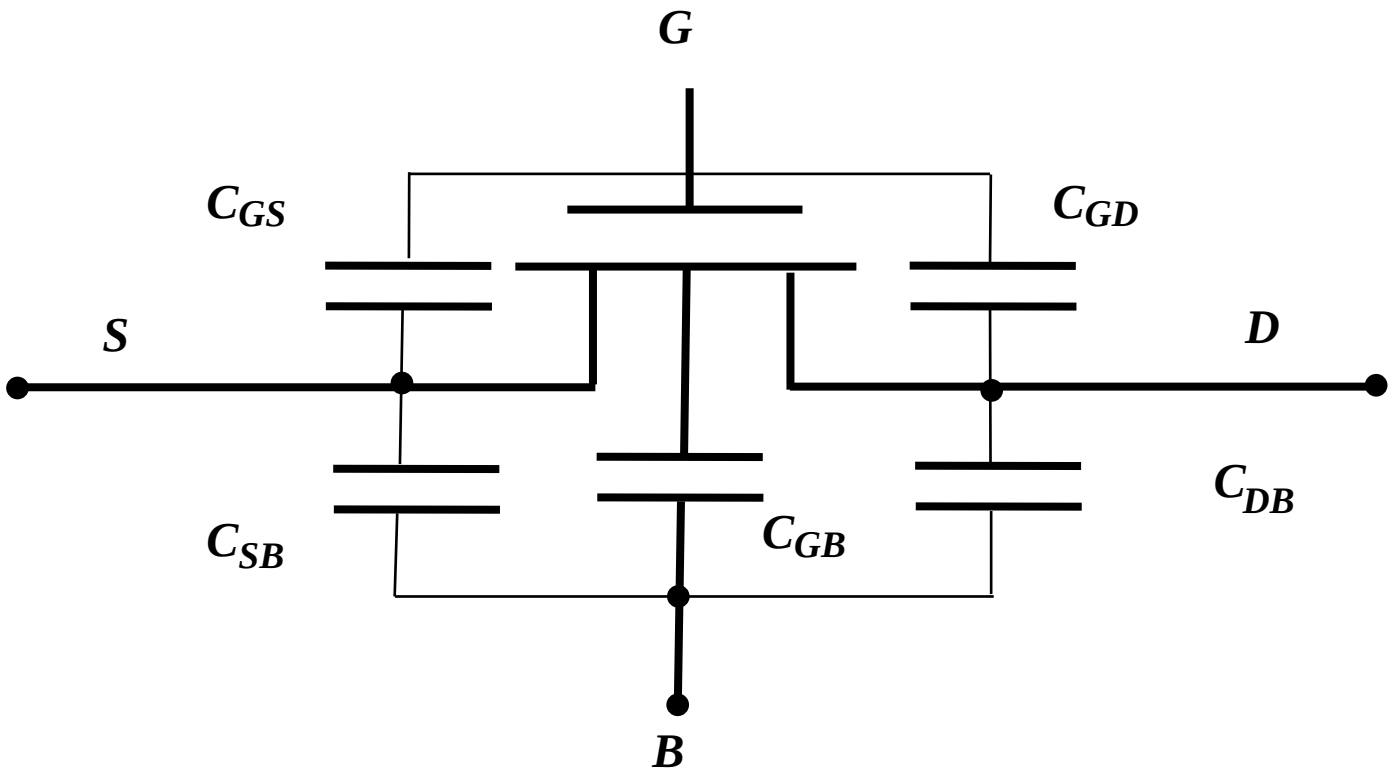
HW3-4

- Please describe the following things:
  - Linear Region of a MOS Transistor
  - Saturation Region of a MOS Transistor
  - Short Channel effect of a MOS Transistor

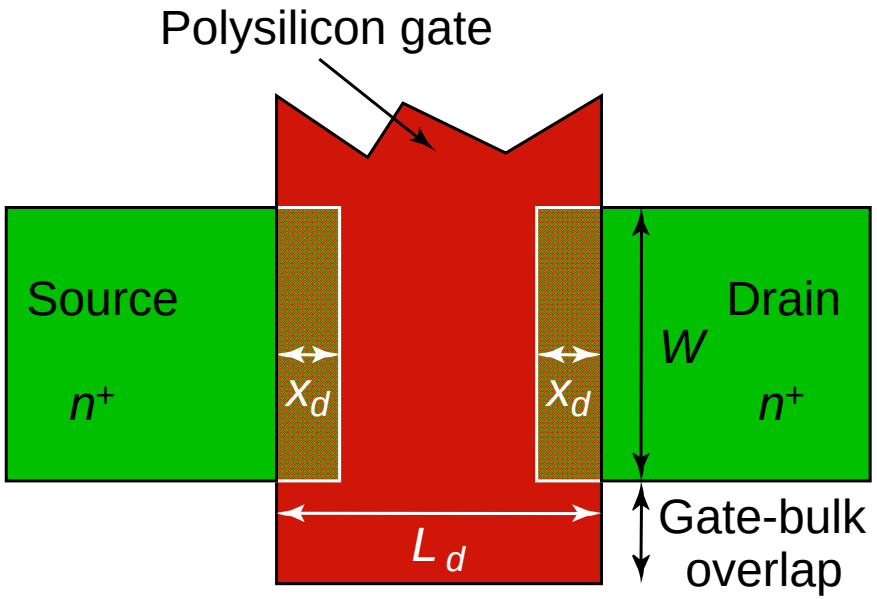
MOS Capacitances Dynamic Behavior

1815 Thomson Map of China & Formosa (Taiwan)

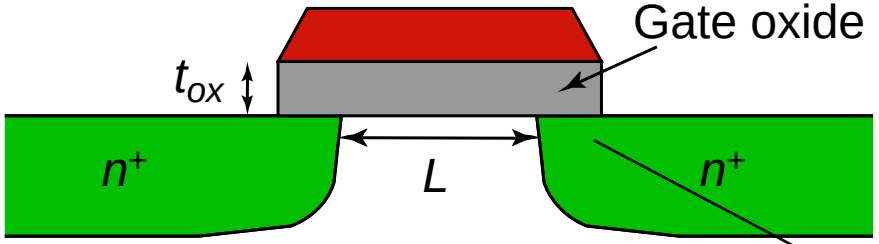
Dynamic Behavior of MOS Transistor



The Gate Capacitance



Top view



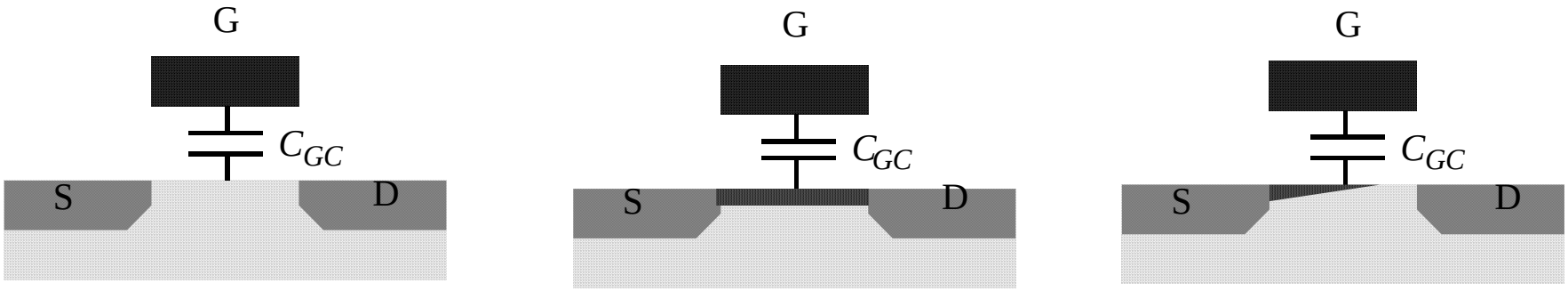
Cross section

$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

Lateral Diffusion

Gate Capacitance

C_{GC}= *Total capacitance*

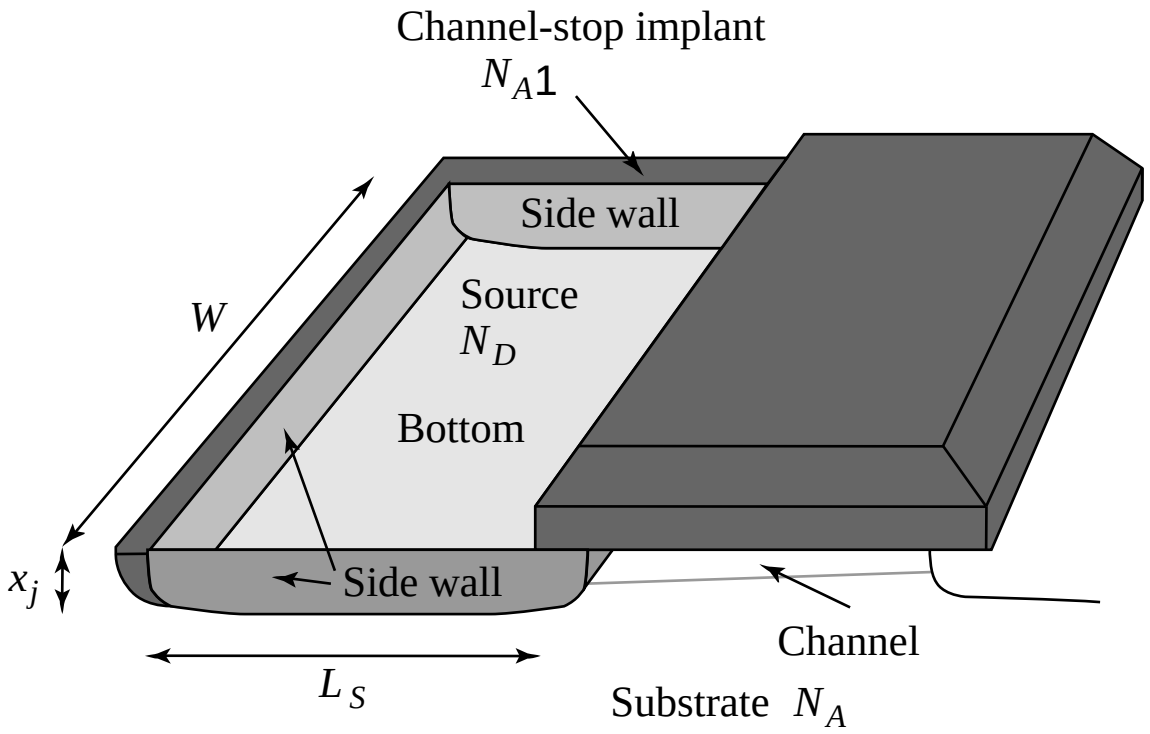


Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Most important regions in digital design: saturation and cut-off

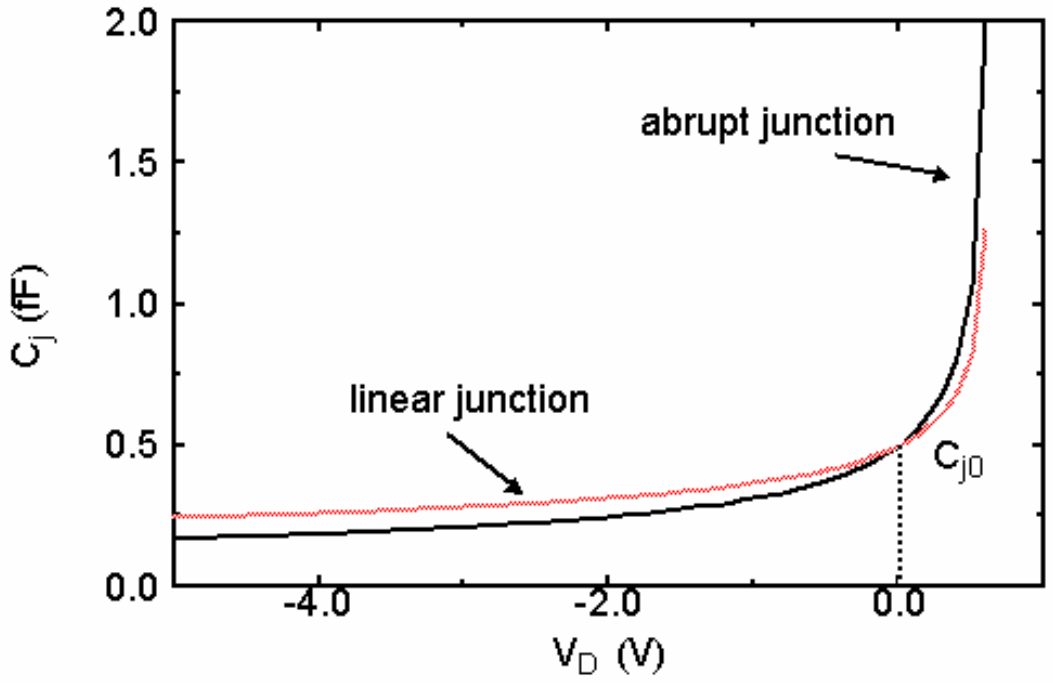
請參考 Text Book: Table 3-4 (Page 109)

Diffusion Capacitance



$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

m = 0.5: abrupt junction
m = 0.33: linear junction

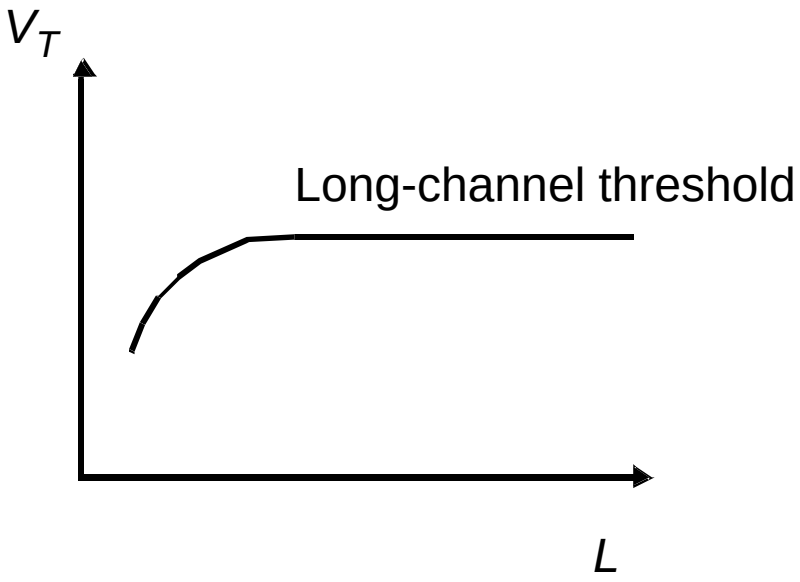
Capacitances in 0.25 μm CMOS process

	C_{ox} (fF/μm^2)	C_O (fF/μm)	C_j (fF/μm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/μm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

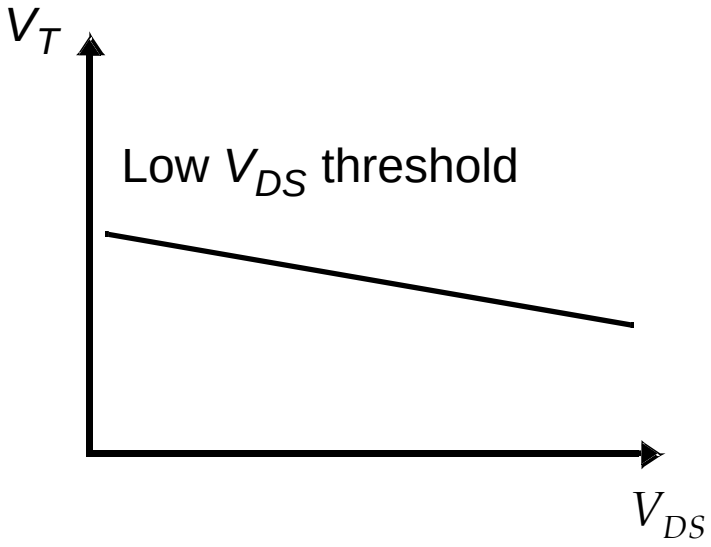
The Sub-Micron MOS Transistor

- **Threshold Variations**
- **Subthreshold Conduction**
- **Parasitic Resistances**

Threshold Variations

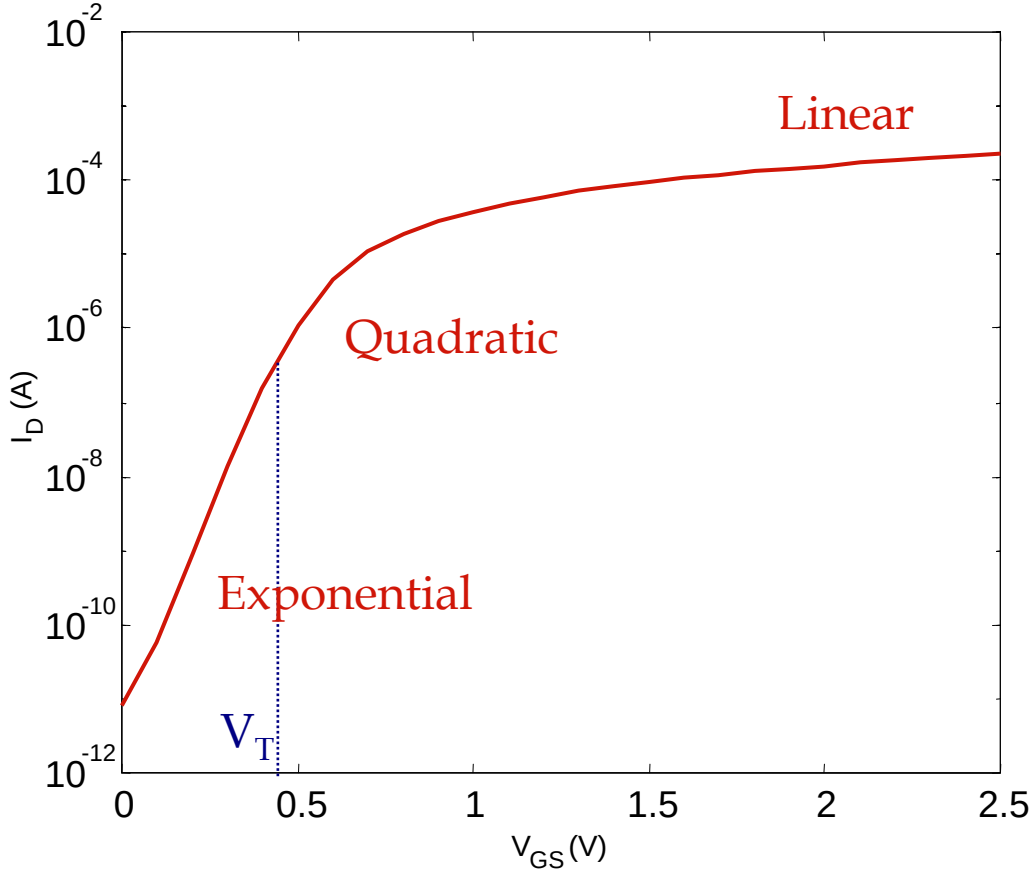


Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (for low L)

Sub-Threshold Conduction



The Slope Factor

$$I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

S is ΔV_{GS} for I_{D2}/I_{D1} =10

Slope Factor

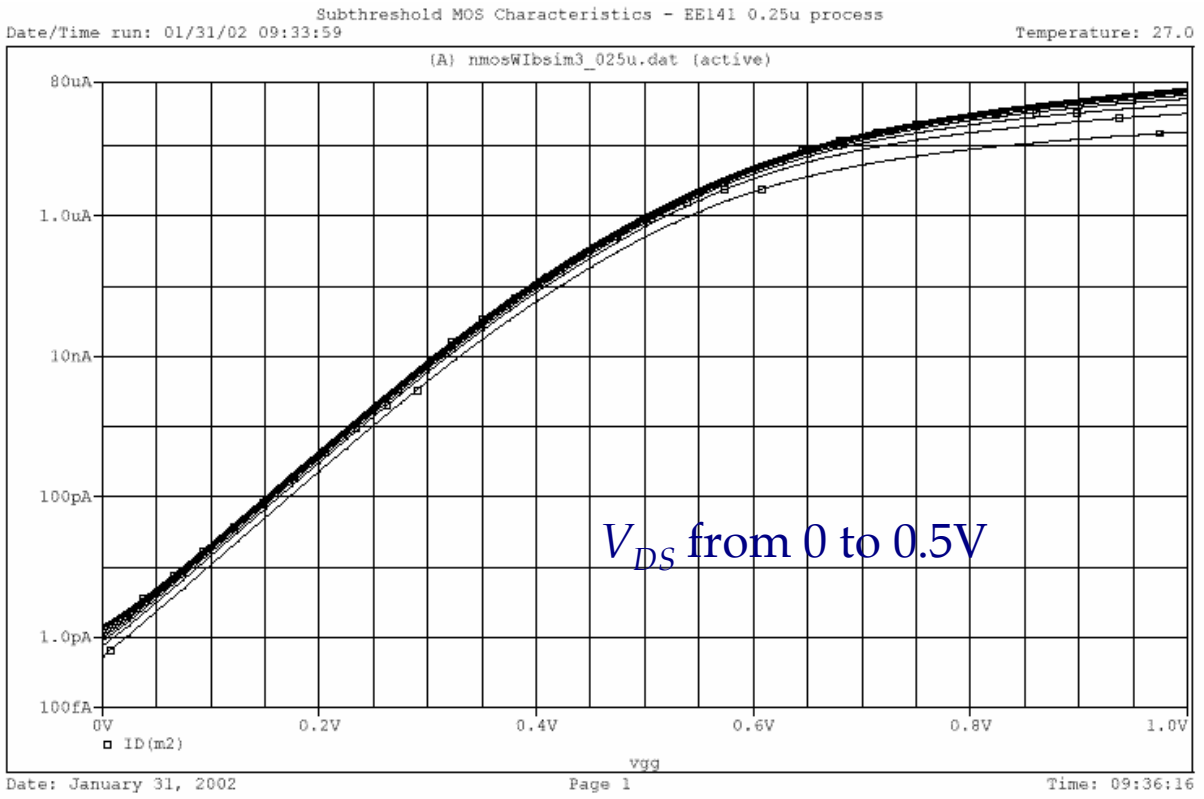
$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

Typical values for S:
60 .. 100 mV/decade

每增加 60 mV, 電流增加10 倍

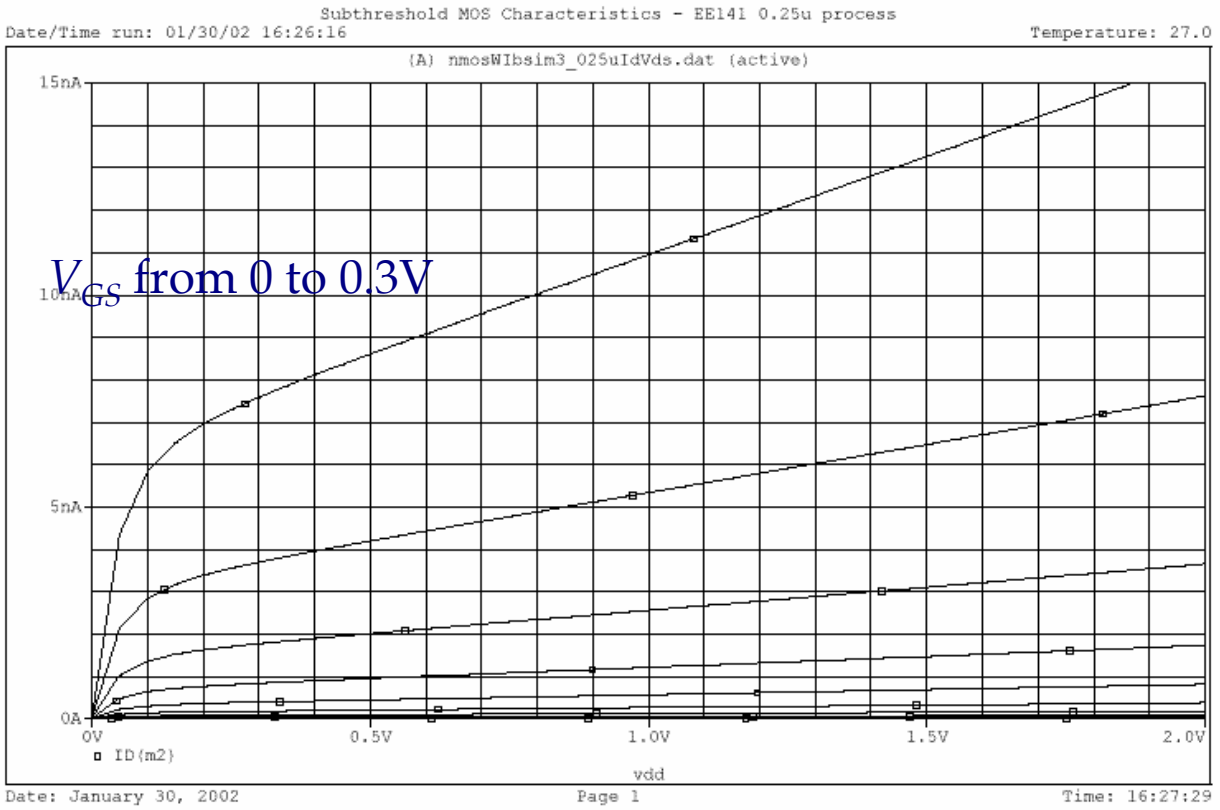
Sub-Threshold I_D vs V_{GS}

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right)$$



Sub-Threshold I_D vs. V_{DS}

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right)\left(1 + \lambda \cdot V_{DS}\right)$$

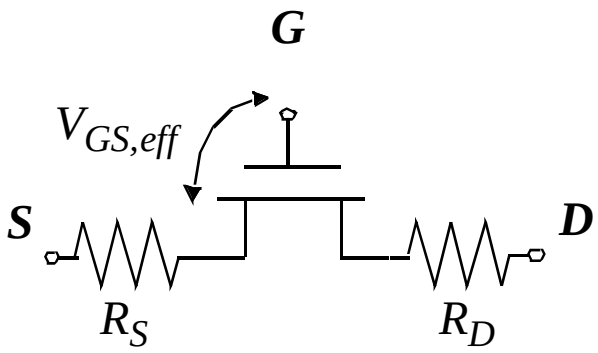


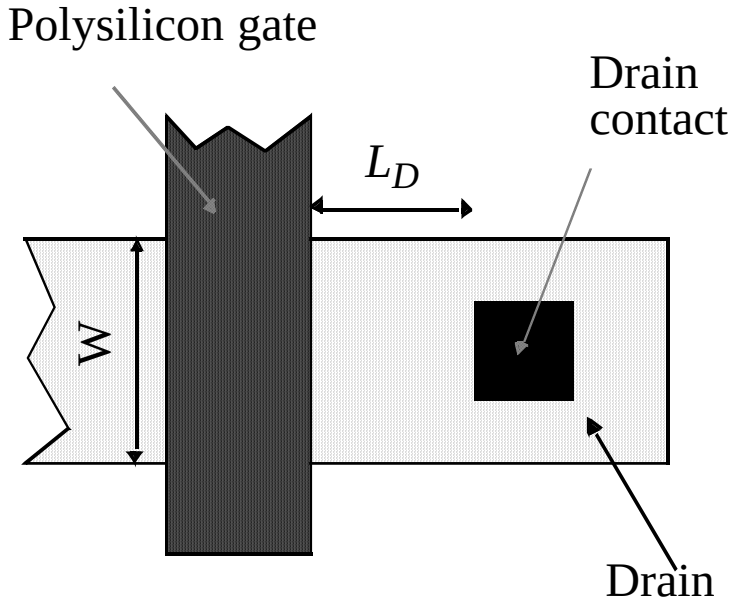
V_{GS} from 0 to 0.3V

Summary of MOSFET Operating Regions

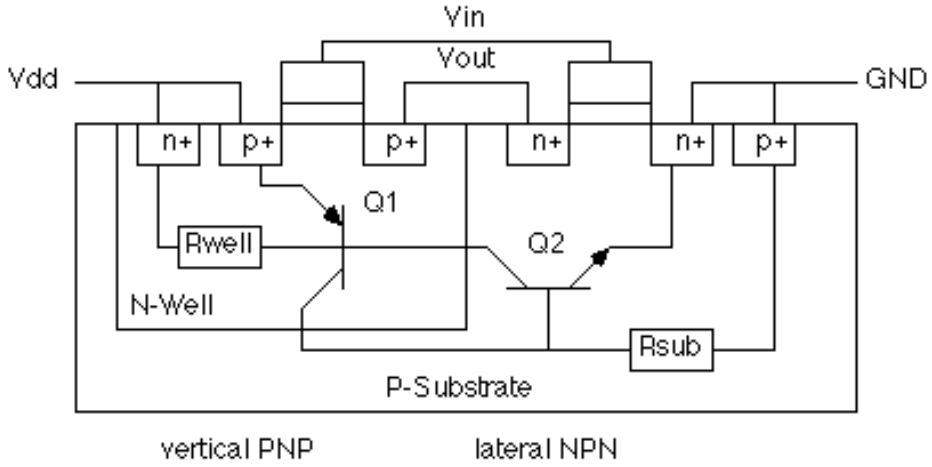
- Strong Inversion $V_{GS} > V_T$
  - Linear (Resistive) $V_{DS} < V_{DSAT}$
  - Saturated (Constant Current) $V_{DS} \geq V_{DSAT}$
- Weak Inversion (Sub-Threshold) $V_{GS} \leq V_T$
  - Exponential in V_{GS} with linear V_{DS} dependence

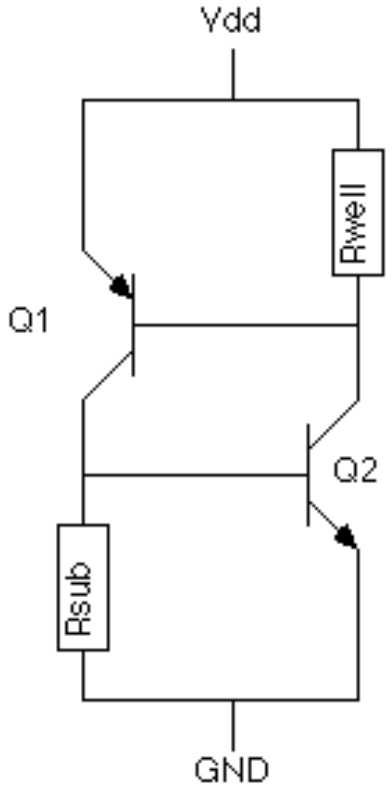
Parasitic Resistances





CMOS Latch-up





若是有來自GND 的 noise spike

→則在 R_{sub} 上會有一暫時性的壓降

→此壓降會使 Q2 的 V_B ↑ → Turn on Q2 → Q2 電流↑

→ Q2 的 current 使 R_{WELL} 上的壓降↑

→此壓降會使 Q1 的 V_B ↓ → Turn on Q1 (PNP)

→此壓降會使 Q2 的 VB ↑

Latch-up in CMOS circuits

- CMOS因爲都是 “Well” process, 這也造成一些無法避免的 junction, 一但有junction, Diode, Bipolar, Resistor 的效應便出現,這些非原先設計的元件會造成V_{DD}與V_{SS}間一個 “low-resistance conducting path”
- Latch-up 的 induce:
  - 1)glitches on the supply rails
  - 2)incident radiation

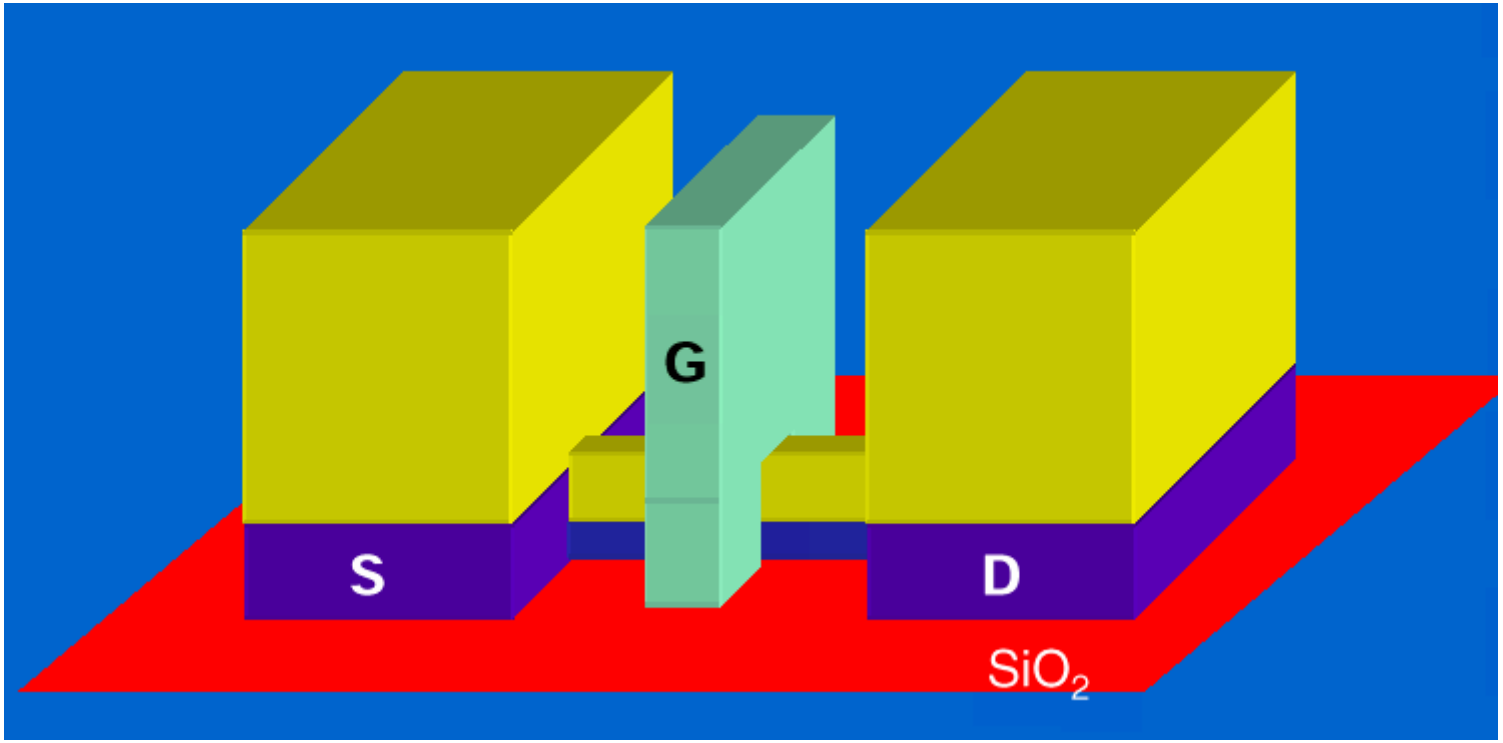
Remedies for the latch-up problem (1/2)

- 提高substrate之doping level, drop the R_s
- Reducing R_{well} by control of fabrication parameters and by ensuring a low contact resistance to V_{SS}
- Guard ring
- Trench Isolation: 利用Dry Etching,在 NMOS 及PMOS間挖一道 Trench,並填 SiO_2
- SOI
- 其它.....

Remedies for the latch-up problem (2/2)

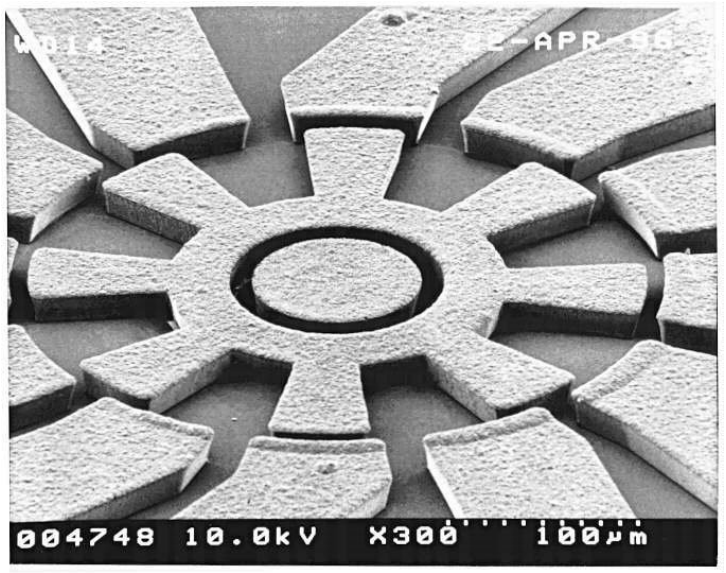
- 每個 substrate 及 well 都要有 contact
- 每個 substrate 及 well 之contact 都要接到 V_{DD} 或 V_{SS}
- 每個 substrate 及 well 之contact 都要儘量接近 source
- 至少每 5 - 10 個 Tr. 要有一個 substrate contact
- n Tr. 要靠近 V_{SS}, p Tr. 要靠近 V_{DD}

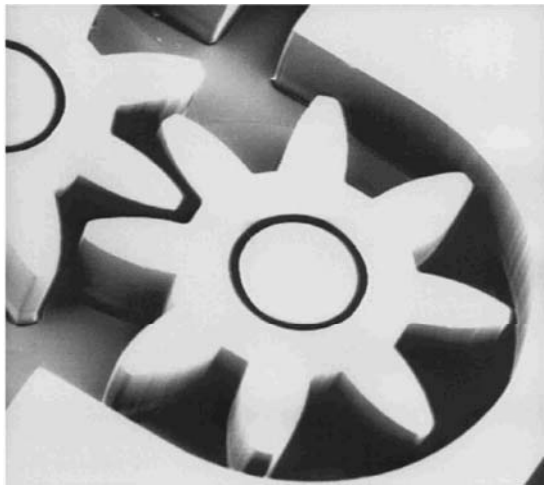
Future Perspectives (1/2)



25 nm FINFET MOS transistor

Future Perspectives (2/2)





HW3-5

- Please describe the facts of:
  - Body Effect
  - Latch-Up
  - The remedies to avoid latch-up effect